Research and Development Technical Report

# COMPUTER AIDED DESIGN OF INTEGRATED CIRCUIT FABRICATION PROCESSES FOR VLSI DEVICES

A SEMI-ANNUAL TECHNICAL STATUS REPORT

February 15, 1980 - August 14, 1980

DARPA Contract No. MDA 903-79-C-0257
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Research Project

# COMPUTER AIDED DESIGN OF INTEGRATED CIRCUIT FABRICATION PROCESSES FOR VLSI DEVICES

ISSUED TO: STANFORD UNIVERSITY
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COMPUTER AIDED DESIGN OF

INTEGRATED CIRCUIT FABRICATION PROCESSES

FOR VLSI DEVICES

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February 16, 1980 - August 14, 1980

# COMPUTER AIDED DESIGN OF INTEGRATED CIRCUIT FABRICATION PROCESSES FOR VLSI DEVICES

Contract No. MDA 903-79-C-0257

## Introduction

This report covers the period February 16, 1980 to August 14, 1980. Its organization corresponds to that of the contract proposal with sections devoted to Thermal Oxidation, Ion Implantation, Chemical Vapor Deposition of Silicon, Materials Analysis and Interface Physics, and Process Model Implementation in SUPREM. In each section there will be a brief description of progress made including difficulties encountered, results obtained with their supporting data, and plans for the future.

## THERMAL OXIDATION

J. Plummer, B. Deal, W. Tiller, R. Razouk, C. Ho, L. Lie, H. Massoud

### A. High Pressure Oxidation

High pressure oxidation of silicon affords a means to grow gate and field oxides on silicon at lower temperatures and/or shorter times than conventional atmospheric pressure oxidation. Improvement on these IC processing factors, time and temperature, are important prerequisites for development of VLSI technology, where three dimensional device sealing calls for stricter control of movement

of previous diffusions. Moreover, it has been reported that oxidation induced stacking faults are suppressed or even eliminated by taking advantage of lower temperatures [1,2]. Stacking fault defects have been associated with leaky junctions. Performance and yield, therefore, would considerably benefit from the use of high pressure oxidation.

One of the major goals of the present program is the development of an advanced process modeling capability. This requires the investigation of the latest technological advances and their incorporation in the present process modeling program. For high pressure oxidation, the kinetics of oxide growth in dry $O_2$ and pyrogenic steam ambients need characterization for both (100) and (111) oriented silicon. The variables under investigation are oxidation temperature, ambient, time, and pressure. Also of importance is the density of oxide charges resulting from the oxidation and differences, if any, in charge density between oxidation at 1 atm and at high pressure.

A commerical "Hipox" unit purchased from Gasonics, Mountain View, California, was utilized to obtain kinetic data for high pressure oxidation. Improvements and modifications were introduced to the system to achieve the more precise control requirements needed for the kinetic studies. Data were obtained for oxidation in a pyrogenic steam ambient at pressures ranging from 1 to 20 atm in the temperature range of 800° to 1000°C. Silicon substrates of (100) and (111) orientation were used. The linear-parabolic model developed by Deal and Grove [3] was used for the analysis of the kinetic data. This model is expressed by

$$x_o^2 + Ax_o = Bt + x_i^2 + Ax_i \qquad (1)$$

which can be rewritten as

$$x_o^2 + Ax_o = B\,(t + \tau) \qquad (2)$$

where

$$B = 2\, D_{eff}\, C^*/N_1 \tag{3}$$

$$A = 2\, D_{eff}\, (1/k + 1/h) \tag{4}$$

$x_o$ = oxide thickness

$t$ = oxidation time

$\tau = (x_i^2 + Ax_i)/B$

$x_i$ = initial oxide thickness such that $x_o = x_i$ at $t = 0$

$D_{eff}$ is the effective diffusion coefficient of the oxidizing species and incorporates any enhancements in the transport rates, C* is the equilibrium concentration of the oxidant in the oxide, $N_1$ is the number of oxidant molecules incorporated into a unit volume of the oxide layer, h is the gas-phase transport coefficient and k is a first-order interface reaction constant.

The general oxidation relationship as summarized by Eqs. (1) - (4) indicates a pressure dependence of both the parabolic rate constant (B) and the linear rate constant (B/A) through their dependence on the equilibirum concentration of the oxidant (C*) in the oxide which is assumed to be related to the partial pressure of the oxidant in the gas by Henry's law: $C^* = KP$, in the case where the oxidants are undissociated molecular species.

To accurately determine the pressure dependence of the rate constant from the actual experimental data, the continuously changing rate constants during pressurization and depressurization times were taken into account. A computa-itonal method suitable for inclusion in SUPREM III was developed which allowed us to determine simultaneous values of B and B/A for the linear-parabolic oxidation model, which would satisfy the experimental conditions of time, temperature, pressure, and ambient of the resulting oxide thicknesses with a typical accuracy of less than ±3%.

The linear parabolic oxidation model can be rewritten for a general oxidation interval

$$\Delta t_i = t_{i+1} - t_i \tag{5}$$

and

$$x_{i+1}^2 + Ax_{i+1} = B_i \Delta t_i + x_i^2 + Ax_i \tag{6}$$

By considering

$\Delta t_1$ = atmospheric oxidation time interval before pressurization

$\Delta t_2$ = oxidation time interval during pressurization

$\Delta t_3$ = oxidation time interval at pressure

$\Delta t_4$ = oxidation time interval during depressurization

The oxide thickness following a high pressure oxidation cycle can be written as

$$x_5 = \frac{1}{2}\left\{-A + \sqrt{A^2 + 4B\left[\Delta t_1 + \left(\frac{P+1}{2}\right)\left(\Delta t_2 + \Delta t_4\right) + P\Delta t_3\right]}\right\} \tag{7}$$

where $x_5$ = final oxide thickness obtained experimentally.

The rate constants obtained are summarized in Figs. 1 and 2, which show that the rate constants are linearly proportional to pressure in agreement with the model predictions. A change in activation energy around 900°C was noted and could be indicative of structural changes in the oxide at these growth temperatures, possibly related to the viscous flow postulated by EerNisse [4,5]. The apparent increase in activation energy associated with the parabolic rate constant below 900°C was noted earlier in atmospheric steam oxidation results [6].

Oxide charge densities were measured and characterized for oxidations at 1, 5, 10, 15 and 20 atm in a pyrogenic steam ambient followed by a 10 minute depressurization cycle/anneal in nitrogen. Fixed oxide charge and interface trapped charge densities were found to be slightly higher at temperatures below 900°C than for oxides grown at 1 atm. Evidence indicates

that these charges were annealable in subsequent heat treatments at temperatures of 900 and 1000°C in argon. (Fig. 3)

These results were presented at the Electrochemical Society Meeting in Hollywood, Florida, and will be the subject of a publication in the same journal.

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[4] E. P. EerNisse and G.F. Derbenwick, IEEE Trans. Nucl. Sci., NS-23, 1534 (1976).

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[6] B.E. Deal, J. Electrochem. Soc., 125, 576 (1978).

### B. Thin Oxide Kinetics and Charges

Charge characterization of the Si-$SiO_2$ interface is accomplished by measuring both the high-frequency and quasi-static CV curves of MOS capacitors made by the metallization of both the front and back sides of the oxidized silicon. The oxide on the wafer back side is removed before the back-side metallization to provide a good contact to the silicon substrate and to reduce the series contact resistance which influences the capacitance measured.

In this time period, second order effects, such as the method of drying the wafer prior to oxidation, the impact of backside damage ion implantation prior to oxidation, pre-oxidation treatment in Ar-HCl and the method of metallization were investigated to determine their effects on capacitor breakdown distribution, backside contact and series resistance, and the $Si/SiO_2$ interface charge properties.

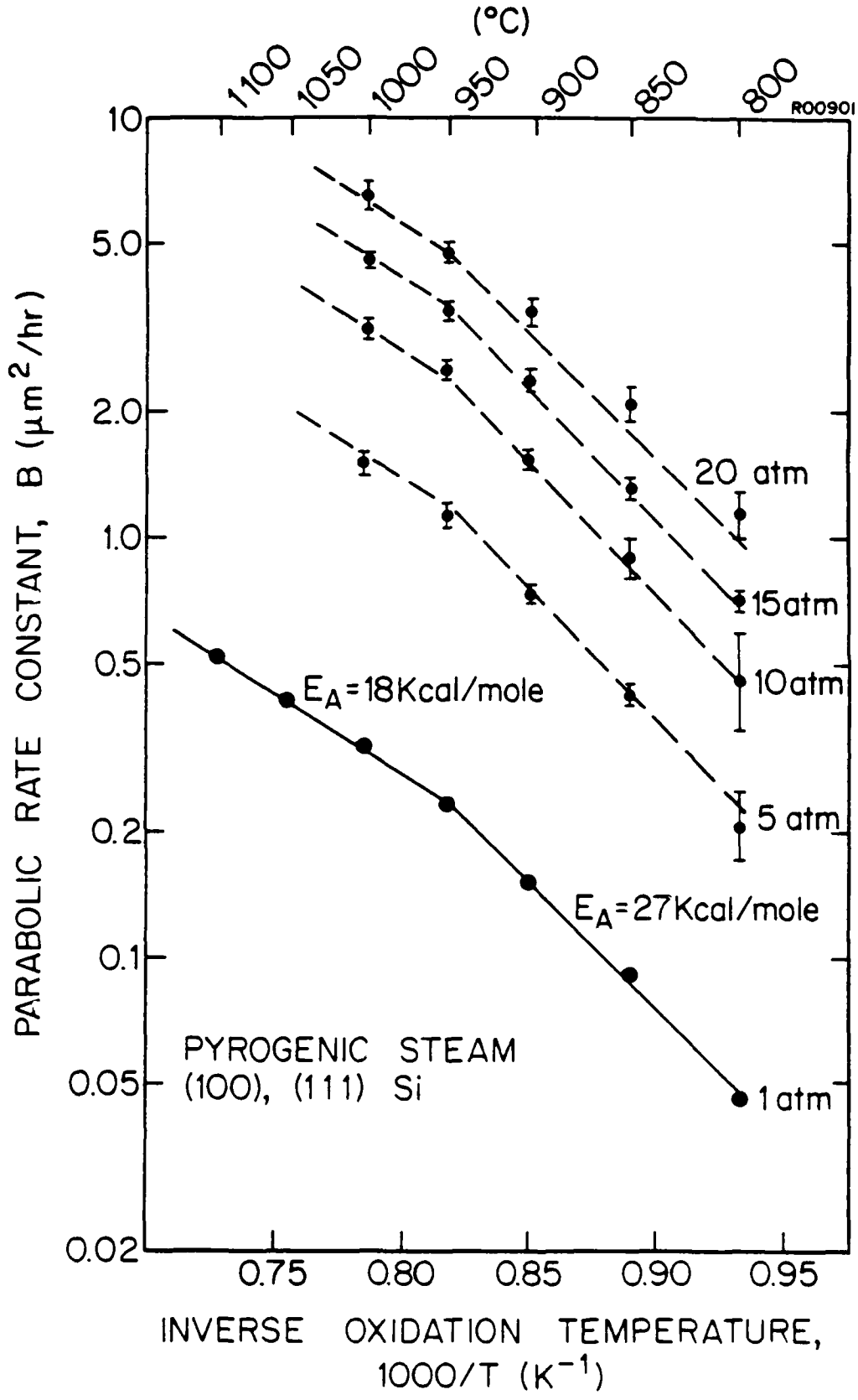


Fig. 1. Parabolic rate constant B versus 1000/T for (100) and (111) silicon wafers oxidized in pyrogenic steam as obtained from data at 1, 5, 10, 15 and 20 atm.

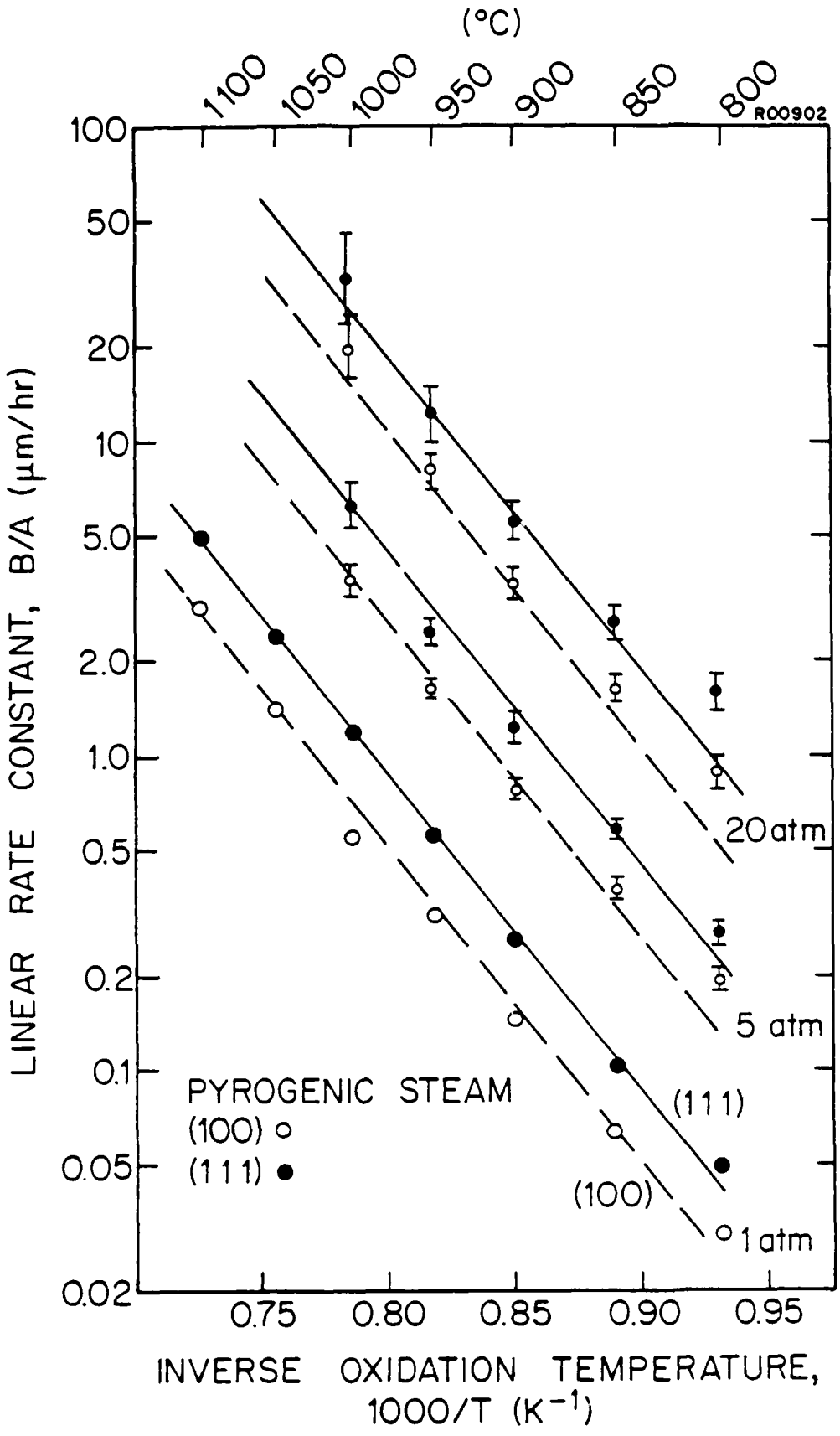


Fig. 2 Linear rate constant B/A versus 1000/T for (100) and (111) silicon wafers oxidized in pyrogenic steam as obtained from 1, 5 and 20 atm data.

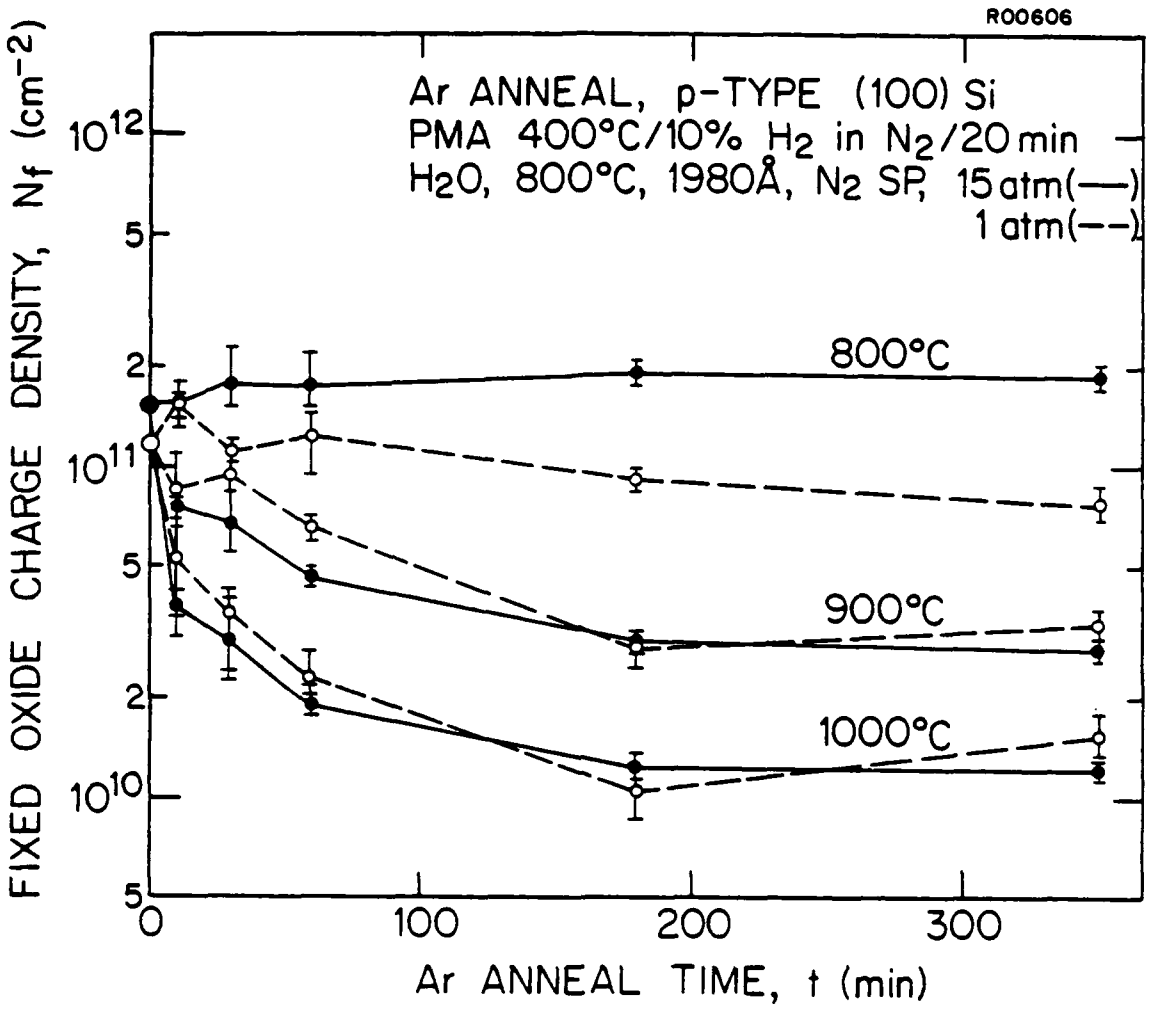


Fig. 3. Fixed oxide charge density versus post-oxidation Ar anneal time. Samples were initially oxidized in steam at 800°C at 1 or 15 atm and subsequently annealed in argon for various times.

1. Wafer Drying: No noticeable differences in oxide thickness, oxide fixed charge density or midgap interface trap density between wafers that were blown dry with a nitrogen gun or dried used boiling isopropyl vapors were found. The isopropyl alcohol technique was subsequently adopted for its additional attractive feature which is that the wafers do not come in contact with filter paper during the drying process.

2. Back-side implant: N-type wafers were implanted on the back side using 100 KeV phosphorus with a $5 \times 10^{15}$ $cm^{-2}$ dose. They were simultaneously oxidized with unimplanted wafers and metallized together to form MOS capacitors. The back side implant did not affect the oxidation kinetics. The oxide thickness measured was identical in both cases. The post metallization anneal reduced the midgap interface trap density to the same minimum in both cases. However, the series resistance was reduced by the backside implant to one third of its un-implanted value. Also, the oxide fixed charge $N_f$ was observed to be dramatically higher in the backside implanted cases. This observation is interesting, although based on a single experiment at the present time and is under further investigation.

3. Metallization - Alloying Effects: Simultaneously oxidized silicon wafers were metallized in an E-beam metallization system and a flash evaporation system. The flash evaporation system was used to avoid the radiation damage that occurs in the E-beam evaporation system. The alloying reaction of $SiO_2$ with E-beam aluminum was found to consume 20 Å more than the flash evaporation case. Since we are interested in studying ultrathin layers of $SiO_2$, the flash system was adopted as the metallization technique.

4. Pre-oxidation treatment in Ar-HCl: One of the principal problems in gathering reproducible data on thin oxide kinetics is the dependence of

growth rates on surface preparation techniques. Published results have shown that growth rates can be substantially altered by changing the chemical cleaning procedure used prior to oxidation.

In an effort to avoid these problems, we have installed an oxidation furnace with several special capabilities. Basically a double-walled quartz tube is used in the furnace with the provision for Ar, $O_2$ and HCl ambients in the region between two tubes. The inner tube has provisions for Ar, $O_2$, low partial pressure $O_2$, $N_2$ and HCl ambients, in any combination. This will permit cleaning and gettering of the inner tube, growth of $SiO_2$ layers in $O_2$, $O_2$/HCl and $O_2$/Ar mixtures as well as inert gas annealing in $N_2$ or Ar. An additional feature is the ability to in-situ clean the silicon wafers in an Ar/HCl ambient prior to thermal oxidation.

Initial experiments designed to characterize the effectiveness of this new furnace were carried out as follows. (100)-oriented wafers were oxidized at 1000°C according to the following sequence:

1. 15 minute pre-heating.
2. Pre-oxidation etch 1% HCl in Ar, 20 minutes.
3. Pre-oxidation argon purge (0-180 minutes).
4. Oxidation in dry $O_2$ for 45 minutes.
5. Fast pull.

Steps 2 and/or 3 were omitted for some of the wafers. Measured oxide thicknesses are shown in Fig. 4. It is seen that pre-oxidation purges of 15 minutes or longer result in the same oxide thickness, therefore a 15 minute period of argon purging is required to flush from the furnace traces of the HCl used in the pre-oxidation etch. Wafers which did not receive any pre-oxidation etch ranged in thickness from 421 to 439 Å and it is believed that variations in the cleaning procedure resulted in this scatter in the data. It can also be noticed that the thicknesses obtained in this case were smaller

than those obtained with the pre-oxidation etch, suggesting that the cleaning leaves a surface film that retards the oxidation reaction slightly.

Oxide fixed charge density $N_f$ measured on these samples was $1.05 \pm 0.05 \times 10^{11}$ $cm^{-2}$ for the pre-oxidation etched samples while the wafers which were not pre-oxidation etches ranged from $1.05 \times 10^{11}$ to $1.60 \times 10^{11}$ $cm^{-2}$. These results demonstrate the importance of using proper in-situ cleaning and subsequent purging to obtain reproducible and representative oxide growth kinetic data as well as charge characteristics.

During this time period, study of the growth kinetics of thin oxide layers also continued. Phosphorus- and boron-doped, (100)- and (111)-oriented silicon wafers were cleaned using a hydrogen peroxide-based cleaning procedure. Wafers were then in-situ cleaned in Ar/HCl, purged in Ar and then oxidized in dry oxygen. The wafers were then metallized in a cold flash evaporation system on the front side. The back-side oxide was then removed using buffered oxide etch followed by metallization on the back side for good contact during the high frequency C-V measurement. After the capacitor dot lithography, a post-metallization low-temperature anneal was done at 420°C for 40 minutes in $N_2$.

No differences were observed in the growth kinetics on N-type and P-type samples whether (100)- or (111)-oriented. Fig. 5 (100) and 6 (111) show the oxidation rate obtained experimentally. Also shown in the oxidation rate dx/dt as calculated form the Deal-Grove general oxidation relationship at 1000°C. The enhanced growth rate for thicknesses less than about 500 Å is apparent in the figures.

Charge characterization at the $Si/SiO_2$ interface is accomplished by measuring both the high-frequency and quasi-static capacitance vs. voltage of MOS capacitors.

Under the assumptions of:

1. No contamination in the cleaning, oxidation or metallization procedures [$\rho(x) = 0$].

2. Proper post-metallization annealing so that the contribution of interface traps is negligible, the high frequency capacitance flat-band voltage is given by

$$V_{fb} = \phi_{MS} - \frac{qN_f}{C_{ox}}$$

$$= \phi_{MS} - \left(\frac{qN_f}{\varepsilon_{ox}}\right) x_{ox} \qquad (8)$$

where the terms have their usual meaning. This results in a straight line plot of $V_{fb}$ vs. $x_{ox}$ in which the intercept is $\phi_{MS}$ and the slope is proportional to $N_f$.

If the maximum allowable error in $N_f$ for a 200 Å oxide is set to 1~2 x $10^{10}$ $cm^{-2}$, the flatband voltage $V_{fb}$ and the value of $\phi_{MS}$ must be accurate to within 15 to 25 mV.

The same matrix of samples used for the 1000°C growth kinetics characterization was used in determination of $\phi_{MS}$. Figures 7, 8, 9, and 10 show $V_{fb}$ vs. $x_{ox}$ for (100), (111), N-type and P-type samples. The values of $\phi_{MS}$ obtained in the different cases are shown in Fig. 11, where $\phi_{MS}$ values given by Deal, Snow and Mead, and by Werner are also plotted for comparison. Our data agrees well with the published results of Deal et al. for (111) samples but disagrees with the published (100) data of Werner.

An ongoing part of our research is aimed at explaining the measured differences between (100) and (111) $\phi_{MS}$ values. Theoretical predictions for this difference are not quantitative and there appears to be some indication in our recent work that this difference may in fact be closely connected with the different oxide charge densities on the two orientations. Nevertheless,

to the extent that the above experimental values of $\phi_{MS}$ are correct, we have extracted values of $N_f$ for the 1000°C oxides described above. Typical results are shown in Figs. 12 and 13.

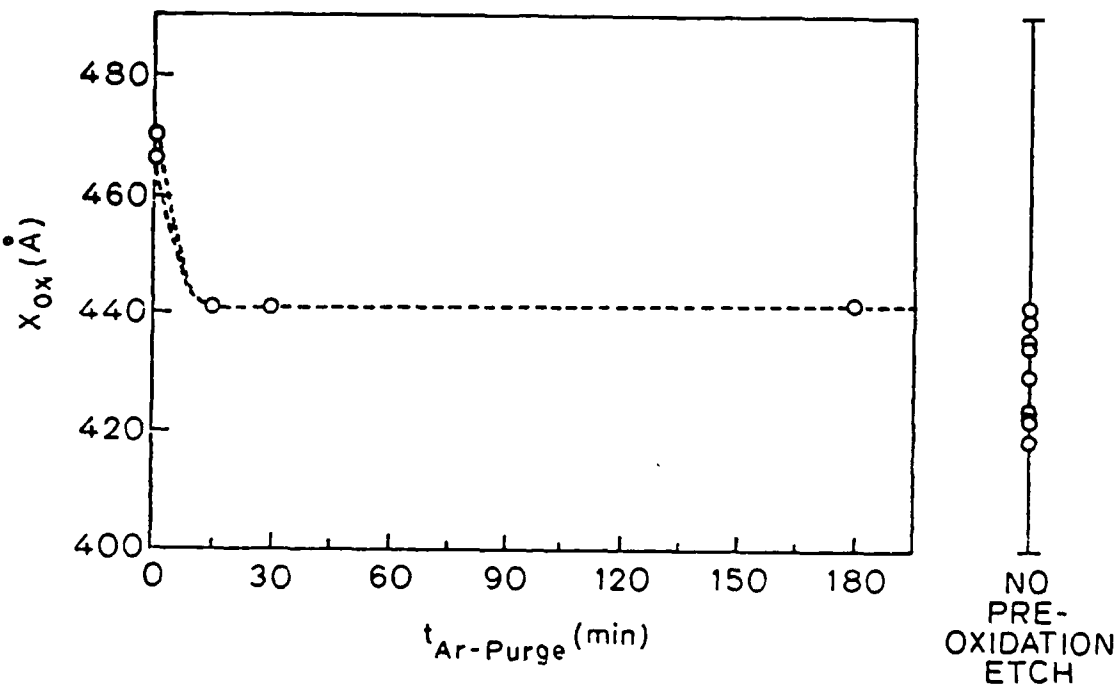


Fig. 4: Effect of preoxidation Ar/HCl etch and Ar purge on the reproducibility of oxides grown at 1000°C for 45 minutes in dry $O_2$, (100) orientation.

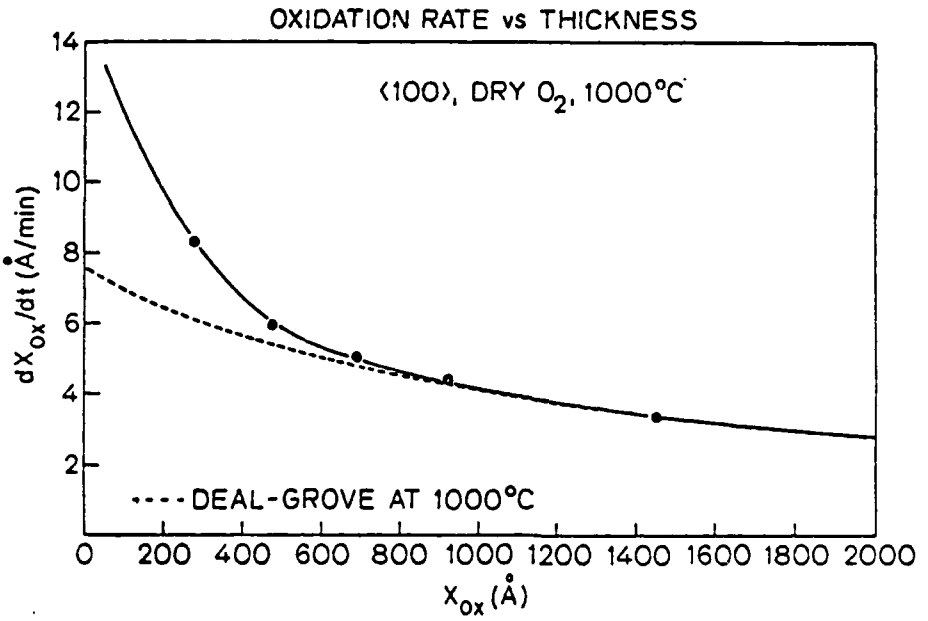


Fig. 5: Oxidation rate dx/dt vs. oxide thickness for (100) silicon at 1000°C in dry $O_2$.

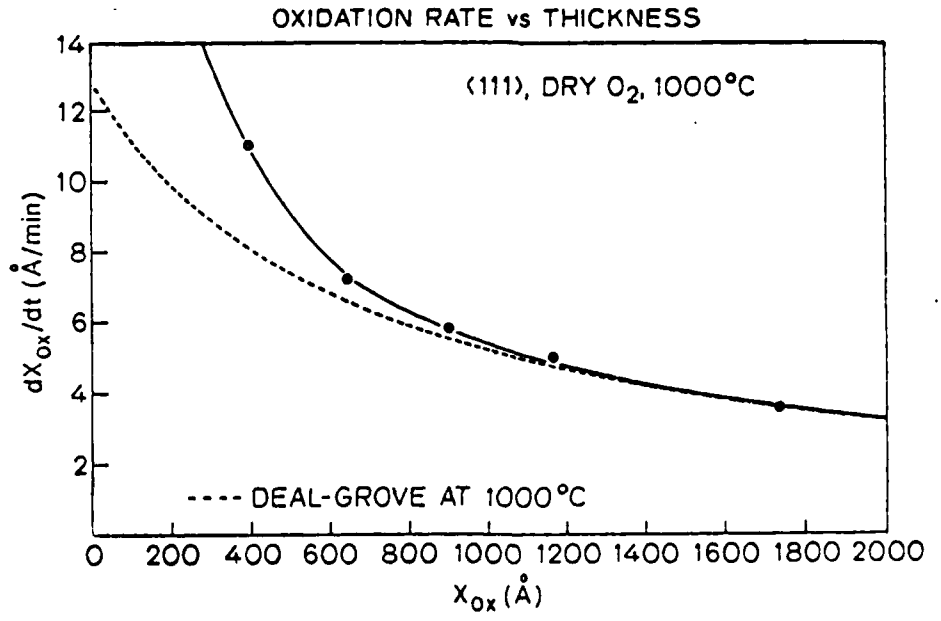


Fig. 6: Oxidation rate dx/dt vs. oxide thickness for (111) silicon at 1000°C in dry $O_2$.

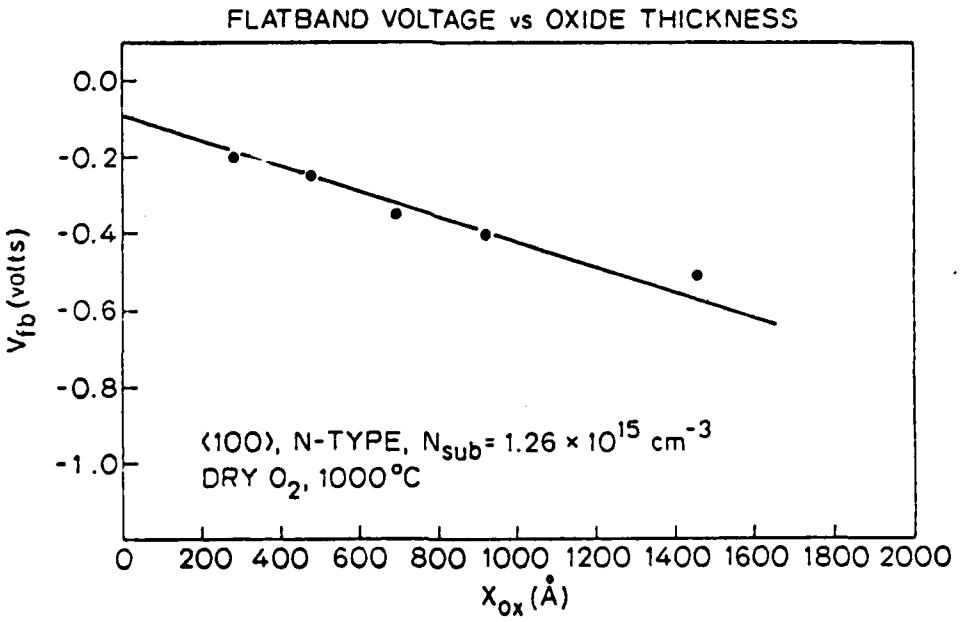


Fig. 7: Flatband voltage vs. oxide thickness for (100) N-type wafers oxidized at 1000 °C and fast pulled from $O_2$ ambient.

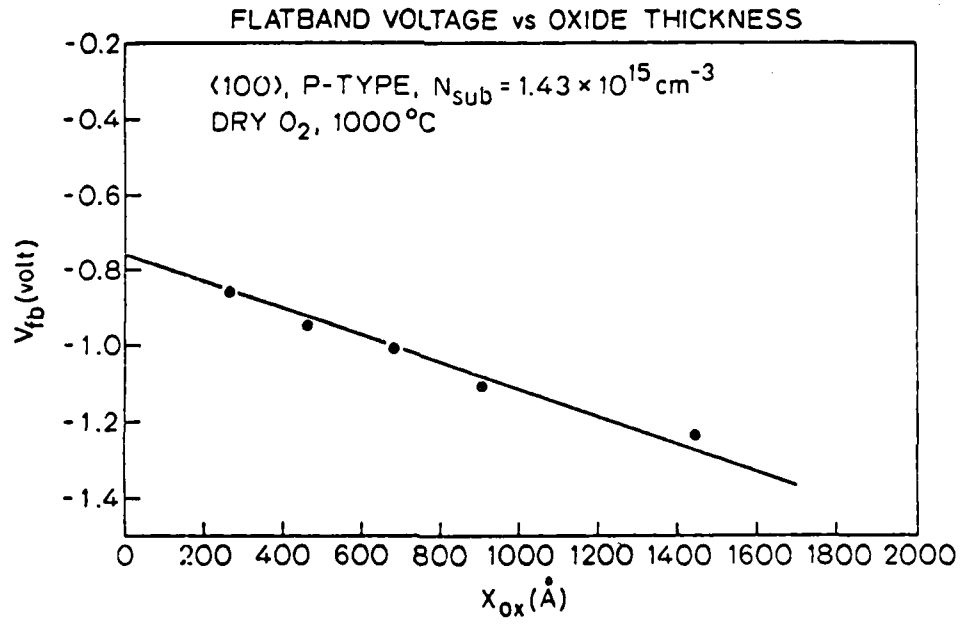


Fig. 8: Flatband voltage vs. oxide thickness for (100) P-type wafers oxidized at 1000°C and fast pulled from $O_2$ ambient.

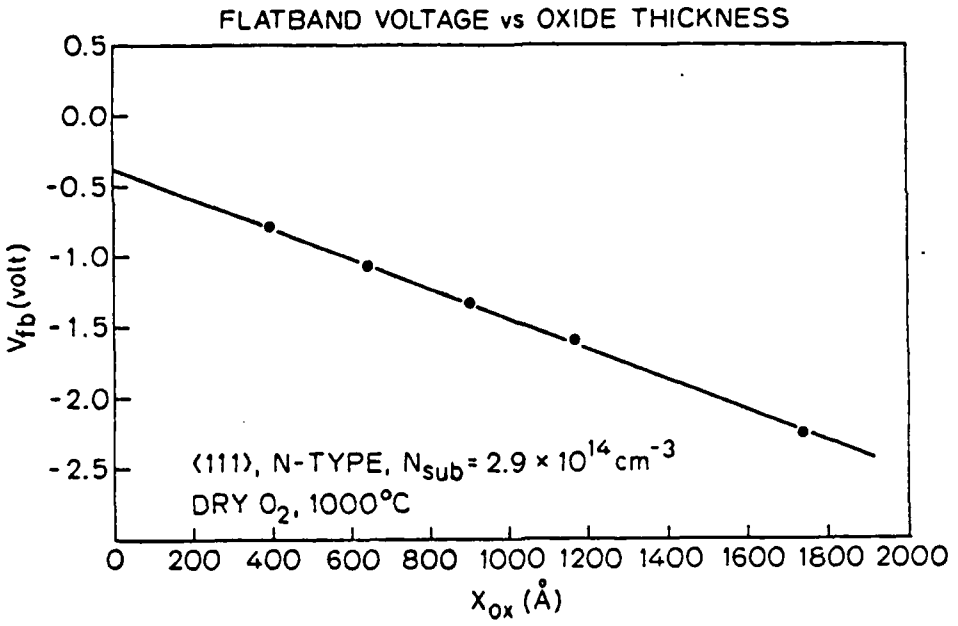


Fig. 9: Flatband voltage vs. oxide thickness for (111) N-type wafers oxidized at 1000°C and fast pulled from $O_2$ ambient.

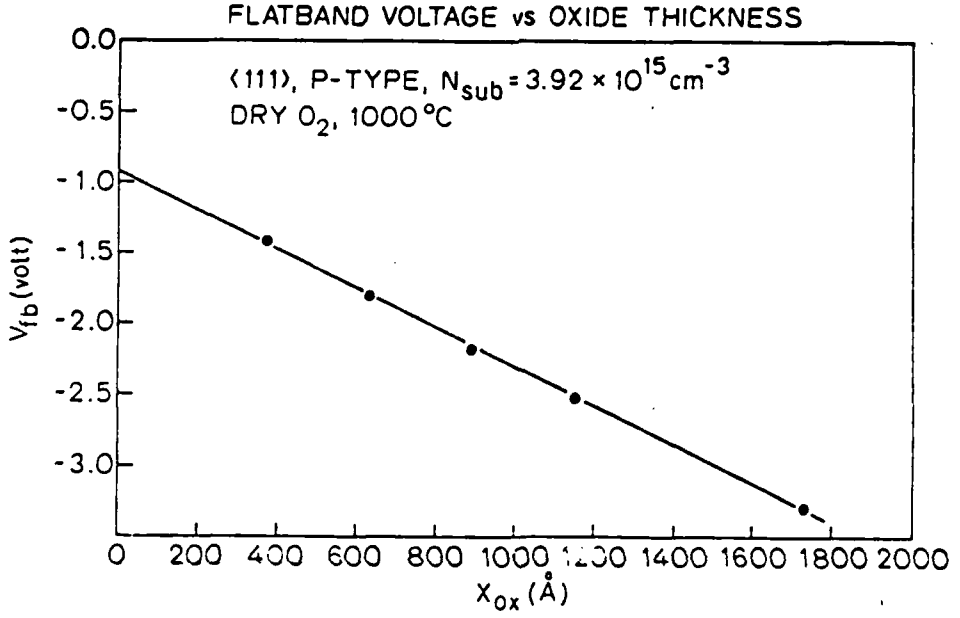


Fig. 10: Flatband voltage vs. oxide thickness for (111) P-type wafers oxidized at 1000°C and fast pulled from $O_2$ ambient.

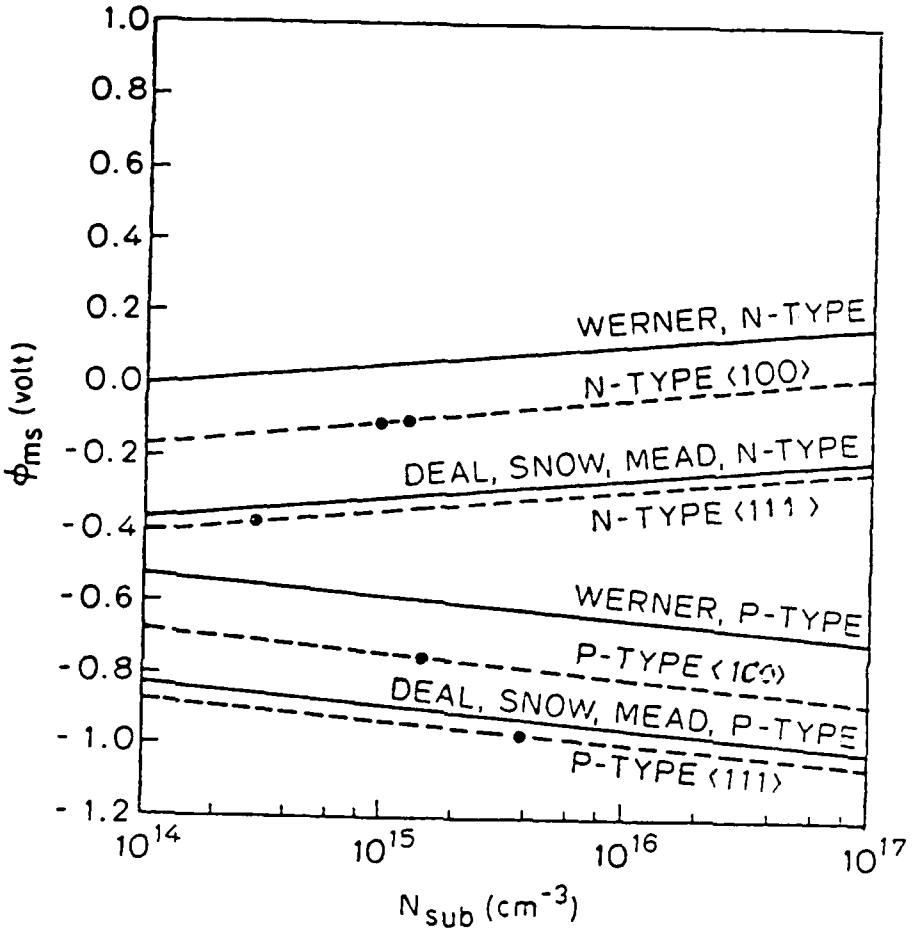


Fig. 11: $\phi_{ms}$ vs. substrate doping for (100) and (111) substrates. The dashed lines correspond to this study.

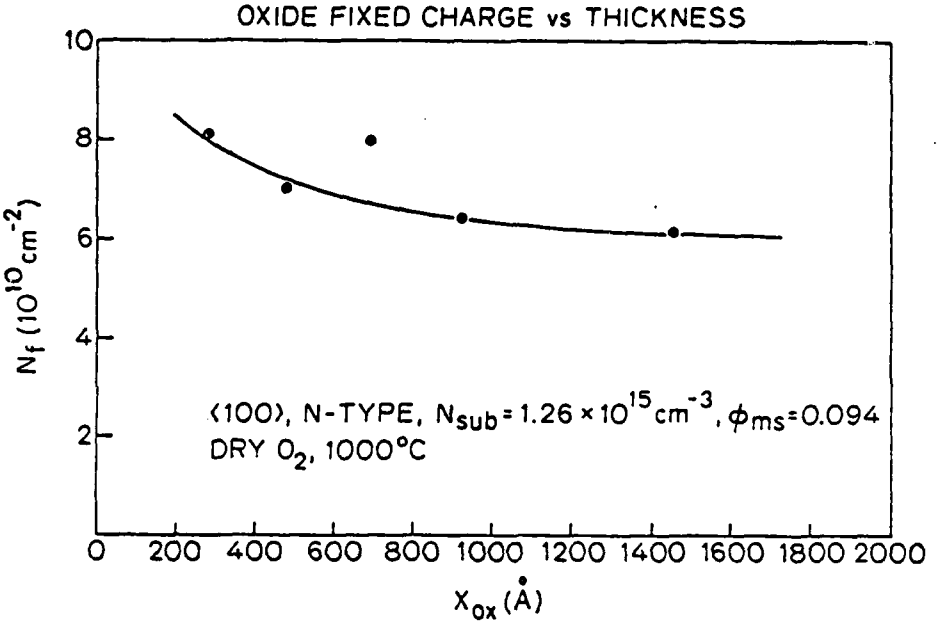


Fig. 12: Fixed oxide charge $N_f$ vs. oxide thickness for (100) N-type wafers oxidized in dry $O_2$ at 1000°C and fast pulled with no Ar anneal.

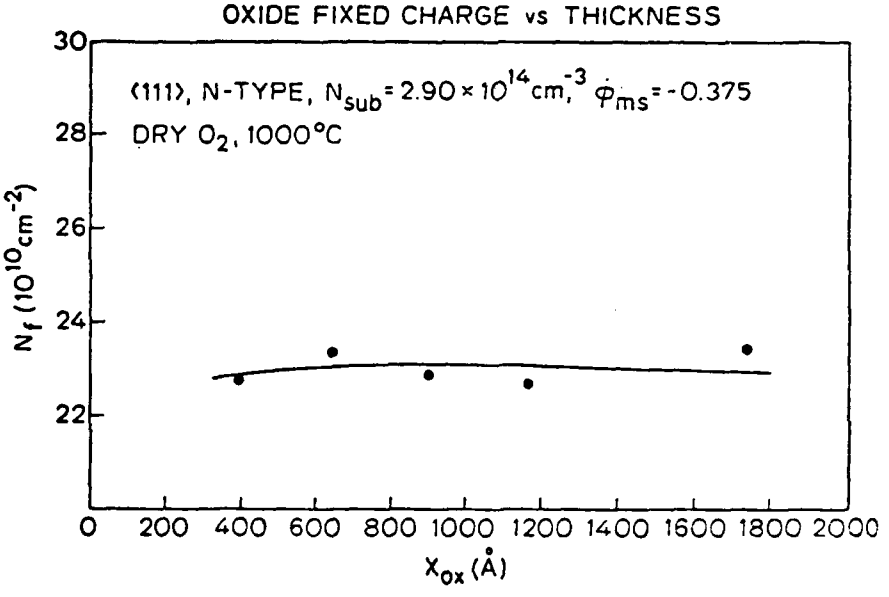


Fig. 13: Fixed oxide charge $N_f$ vs. oxide thickness for (111) N-type wafers oxidized in dry $O_2$ at 1000°C and fast pulled with no Ar anneal.

C. Physical Modeling of the Oxidation Process

Quantitative analysis was made of the Si → α-cristobalite vitreous $SiO_2$ model of thermal oxidation and the chemical potential of interstitial Si defects in each phase has been formulated. The effect of this high concentration of interstitial Si on the annihilation of vacancies has been considered and a condition determining the ambient vacancy concentration, $n_v$, and their chemical potential, $\mu_v$, developed. These considerations shed light on the kinetics of exhaustion of the vacancy sources in the silicon wafer during oxidation.

Having defined the chemical potential for Si interstitials in both Si and $SiO_2$, an equilibrium partition coefficient between the two phases can be calculated. More importantly, the partition coefficient, $k_I$, has a strong oxidation velocity dependence due to the differential activation barriers between the two phases. A plot of $k_I$ versus the number of $Si_I$ defects per unit cell of the Si phase at the interface, $n_{I_1}(0)$, is given in Fig. 14. In the same plot, the number $n_{I_2}(0)$ of $Si_I$ defects in the α-cristobalite unit cell at the interface is given (here, Si and $SiO_2$ ≡ subscript 1 and 2, respectively, and $n_{s2}$ is the number of possible interstitial sites in $SiO_2$).

For approximation that $n_{I_2}(0) \simeq 4$, the excess free energy stored in I-defects, $\Delta G_E$, is given by

$$\Delta G_E \simeq kT \left\{ 4 \ell n (4n^*_{I_2}) + 11 \ell n (11/15) \right\} \qquad (9)$$

where $n_{S2} = 15$ and $n^*_{I_2}$ is the equilibrium concentration of $Si_I$ interstitials in $SiO_2$ in the presence of no excess oxygen. Thus, if $n^*_{I_2} = 10^{-2}$, $10^{-4}$, or $10^{-6}$ per unit cell, $\Delta G_E \simeq$ 6.4, 12.4, and 18 Kcal/mole, respectively.

A quantitative expression was also developed for the flux of $Si_I$-defects into Si from the oxidizing interface. If we neglect annihilation events between the I-defects and the Si vacancies or any interstitial sinks such as

stacking faults, etc., then the concentration, $n_{I_1}$ (0) builds up according to $t^{1/2}$ (here the subscript 1 refers to the Si phase) and the bulk Si also builds up with this time law. This law will thus apply at short times. Allowing annihilation events with vacancies reduces $n_{I_1}$ very little; however, after $n_{I_1} \geq n^*_{I_1}$ for the nucleation of stacking fault loops, a significant sink is present and then $n_{I_1}$ (0) builds up as $t^p$ where $p < 0.5$.

Application of the $Si_I$-defect formation model to the growth and retrogrowth of Si stacking faults followed. This general model allows one to understand the fault size dependence on time, temperature and orientation. Using the two-stream oxidation approach, the time exponent in the growth rate of OISF has been calculated to agree with the experimental value. Oxygen pressure dependence, activation evergies for growth and retrogrowth, plus retrogrowth times and temperatures, have all been determined.

The point to plane corona discharge system with focusing plate has been constructed so that it can be used in conjunction with a standard diffusion furnace. The apparatus is fashioned from quartz to fit into a 106 mm furnace tube and consists of three vertical tiers: the lowest to support the sample, the middle to support the ion focusing plate and the top to support the emitter electrode. Each level is electrically separated form the others by sapphire standoffs which minimize the leakage currents that occur at high temperatures. Special electronic circuitry was needed to control the two important electrical system parameters; i.e., focusing plate voltage and emitter current.

A new project was initiated on the thermal oxidation enhancement of silicon wafers by UV radiation (OEUVR). The first step was a literature synthesis which brought together a comprehensive picture of how $O_1$, $O_2$ and $O_3$ react to electromagnetic radiation in the UV energy system. A general energy level

diagram for the various oxygen processes has been assembled and is presented in Fig. 15. There is a significant absorption in the UV by $O_3$ for $\lambda \lesssim 3000$ Å and by $O_2$ when $\lambda \lesssim 2424$ Å.

To test the feasibility of oxidation enhancement by UV radiation (OEUVR), a simple apparatus was designed and constructed to deliver a wideband UV flux to a Si wafer oxidizing at 900°C. This was achieved by means of a custom, high UV transmitting, "light pipe" arrangement designed for great experimental flexibility. A [111] Si wafer of semicircular shape was mounted perpendicular to the tube axis in the oxidation furnace while a 0.01 meter diameter, 1 meter long $SiO_2$ light pipe was mounted inside and parallel to the tube axis on the downstream side. A $10^{-3}$ m gap existed between the pipe and the wafer surface. The unirradiated portion of the split wafer surrounding the irradiated spot served as the control during a 900°C, 2 hour oxidation in pure oxygen. Because the mere physical presence of the light pipe at that proximity to the wafer obstructs the oxygen flow in the small gap and cools (via the light pipe), the Si surface immediately adjacent to the light pipe, it was also necessary to determine the variation of oxide thickness with location in the unirradiated case. It was found that the oxide was 15% thicker in the non-gap regions of the surface relative to the gap region when no UV radiation was used. When light from a medium intensity wide band UV source was transmitted through the pipe, a 20% increase in oxide thickness was observed compared to the control area (400 Å versus 335 Å).

## ION IMPLANTATION

G. Bronner, L. Christel, J. Gibbons, C. Ho, S. Mylroie, J. Plummer

### A. Boltzmann Transport Modeling of Range Statistics

At the beginning of this time period, the Boltzmann simulation program was well developed and could calculate primary and recoil atom range

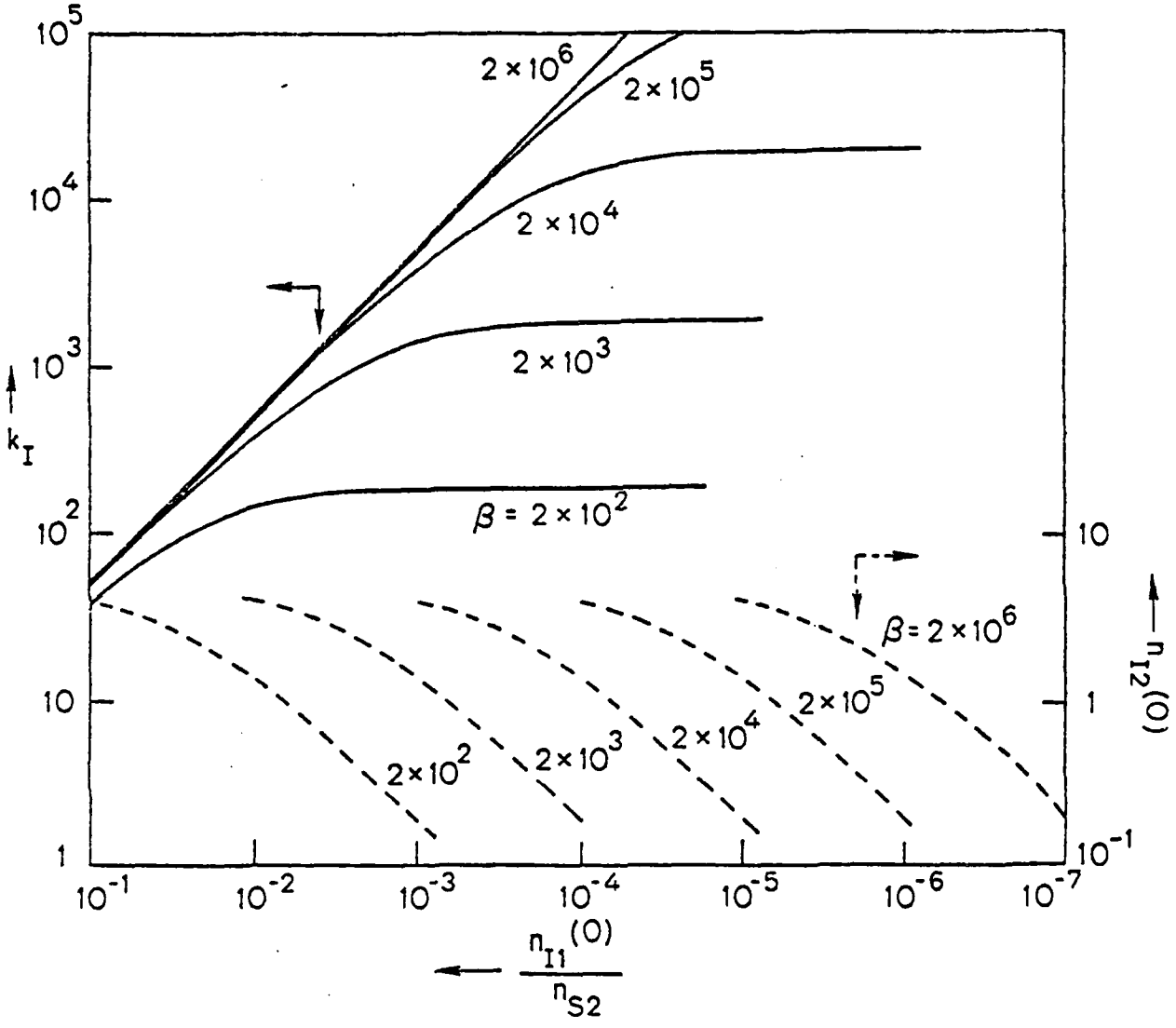


Fig. 14: Plot of the partition coefficient $k_I$ verses the number of $Si_I$ defects per unit cell of the Si phase at the $Si/SiO_2$ interface.

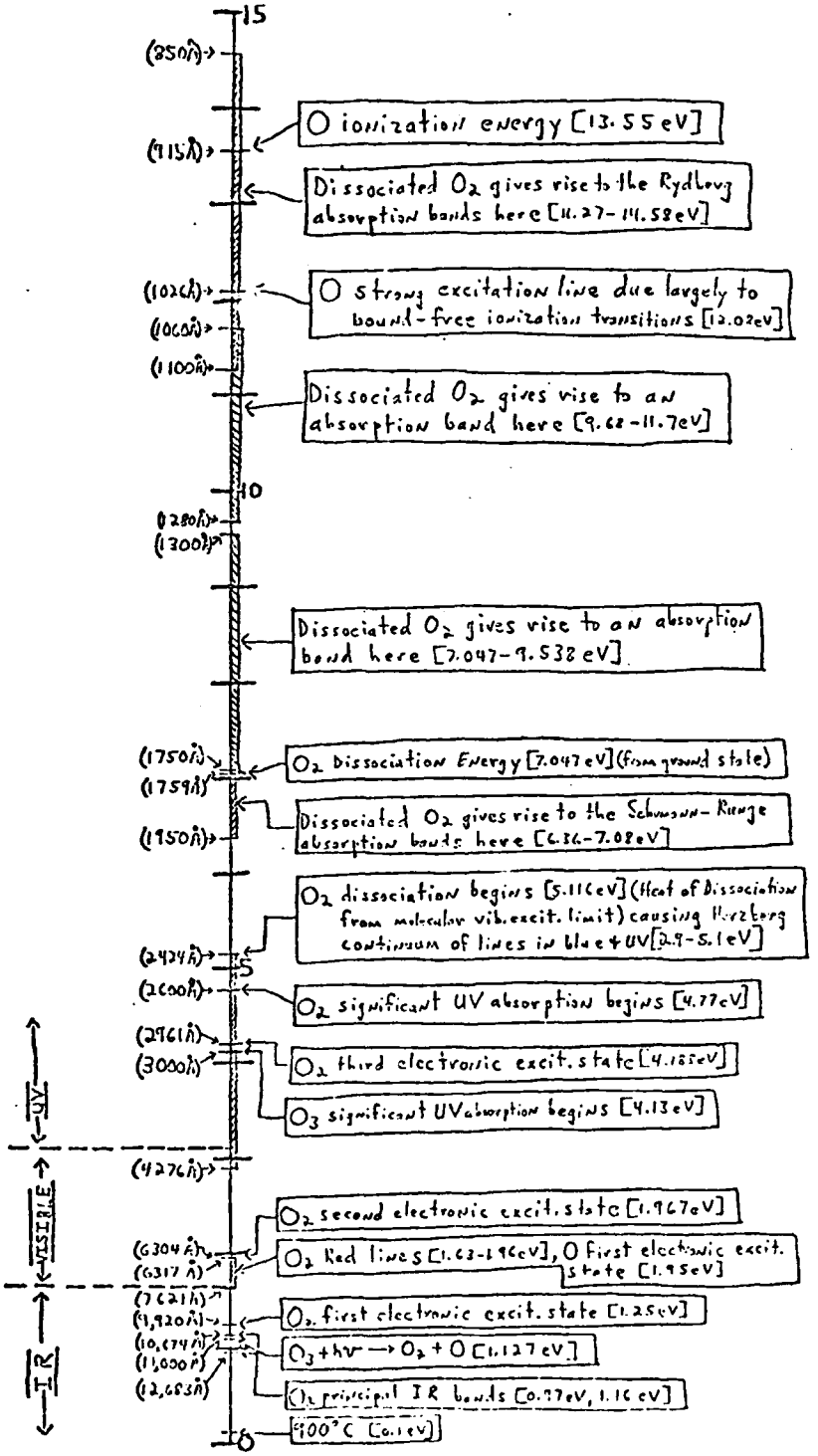


Fig. 15. Energy level diagram for the various oxygen processes possible in OEUVR.

distributions damage density distributions and other recoil effects such as stoichiometry disturbances in compound solids. The execution time of the program had been improved considerably over previous versions and is now believed to be pretty well optimized within a reasonable framework of computational accuracy.

The bulk of this time period was used in a detailed study of recoil range distributions in multilayered targets. It is observed in general that recoil range distributions are characterized by three distinct spatial regions:

(1) A region of very high concentration near the interface.

(2) A region at intermediate depths which is well approximated by an exponential function.

(3) A region of rapidly decaying concentration at a depth about equal to the projected range of a recoil of maximum energy.

Region (1) is understood in terms of the scattering cross section. The cross section is strongly peaked at low energies and hence the largest number of recoils are produced at the lowest energies. These recoils in turn have a high probability of producing more recoils in what is commonly referred to as a cascade process. Thus extremely large numbers of low energy recoils are produced at each point in the thin film. When the interface occurs, these recoils enter the substrate and are stopped quickly, thus producing the high concentration region near the interface.

At present there is no simple theory which predicts an exponentially decaying recoil distribution which would be consistent with region (2). The calculations show that this region contains recoils which originate with about equal probability at each point within the surface film. Thus in this region there are contributions both from high energy recoils produced far from the interface as well as lower energy recoils produced nearer the interface.

Region (3) is simply a manifestation of the fact that there exists a maximum energy $\gamma E_0$ which a recoil atom may attain. Here $E_0$ is the incident beam energy and $\gamma$ is a kinematic factor given by

$$\gamma = \frac{4M_1M_2}{(M_1 + M_2)^2} \tag{10}$$

where $M_1$ and $M_2$ are the ion and recoil mass.

The existence of the exponential region (2) in the calculated recoil distributions prompted a systematic study of the energy, ion and film thickness dependence of oxygen recoil distributions for the important case of the common silicon dopants boron, phosphorus and arsenic incident on silicon targets coated with films of $SiO_2$. Film thicknesses of 500, 750 and 1000 Å of $SiO_2$ were assumed. For each film thickness and ion, four energies were selected in such a way that the projected range of the ion fell one standard deviation before the interface, at the interface, one standard deviation after the interface or at twice the film thickness.

For each of the 36 calculations, a function of the form

$$C(x) = Ae^{-x/L} \tag{11}$$

was fit to the central region of the oxygen recoil distribution. Here C(x) is the concentration of recoiled oxygen at distance x from the interface. When the resulting values of A and L were examined it was found that to a good degree of approximation the relations

$$L[\text{Å}] = 3.75\ \gamma E_0[\text{keV}] \tag{12}$$

$$\frac{A\gamma t_{ox}}{1000\ \text{Å}} = \Phi_0 \cdot 8.7 \cdot 10^4 \exp \frac{-\ln\left(\frac{R_p}{t_{ox}}\right)^2}{0.51} \tag{13}$$

described the exponential regions. Here $t_{ox}$ is the oxide thickness, $\Phi_o$ is the incident dose in $cm^{-2}$ and $R_p$ is the projected range of the incident ion in $SiO_2$. Thus the decay length L is a function only of the maximum recoil energy $\gamma E_o$, independent of ion type or film thickness.

These results were presented in a paper entitled "Recoil Range Distributions in Multilayered Targets" which was presented at the Ion Beam Modifications of Materials conference (IBMM-80) held in Albany, New York in July. The good agreement between calculated distributions and the experimental results of Hirao [7] and Goetzberger et al. [8] were also pointed out in the paper. This paper will appear in the proceedings of the conference which are to be published in a special issue of Nuclear Instruments and Methods in January, 1981.

The remainder of this time period has been spent beginning experiments of our own in an attempt to verify more of the calculated results of the program. Thin films of gold and silver on silicon are being studied because of the ease with which these elements may be detected by Rutherford backscattering. This work will probably form the bulk of our studies over the next few months.

B. Silicide Technology/Transient Process Kinetics

In integrated circuits processing the annealing steps associated with ion implantation are poorly understood. After an implantation, one must anneal the damage created by the implant and electrically activate the implanted dopant. How these processes interact, and how they affect nearby diffusions or oxidations is not known. During this period applications of tungsten silicide ($WSi_2$) to the study of such transient process kinetics has continued.

$WSi_2$ when used as an electrical contact and interconnect is well suited for the study of time-dependent phenomena. It has a very high melting point

and good resistance to the chemicals typically used in I.C. processing. Thus, by using $WSi_2$ as the metal layer, one should be able to first heat cycle and then electrically measure a single device or test structure repeatedly. The time dependence of a process can be studied with a single sample, rather than multiple wafers with their unavoidable and undesirable sample-to-sample variation.

We have completed a series of experiments on MOS capacitors using $WSi_2$ as the metal layer. By commonly accepted MOS parameters ($Q_f$, $D_{it}$, $\Delta V_{FB}$ under bias temperature stress), they were indistinguishable even after repeated heat cycling from uncycled devices using aluminum as the gate electrode. Other workers have reported that residual stress in the silicide films can crack the MOS thin oxide layer [9], but such failures were not apparent in our structures.

Certain test structures for transient process characterization also would employ $WSi_2$ for directly contacting the silicon substrate as in active devices incorporation implanted junctions. A potential problem might be diffusion of free tungsten in the $WSi_2$ into the silicon to act as a deep level trap and therefore perhaps increase the junction leakage currents. Experimental $WSi_2$/Si contacts, however, did not appear to exhibit degradation of junction leakage.

Additional experiments were begun to address other aspects of $WSi_2$/Si contacts and their potential influence on p-n junction behavior. These include contact resistance, reliability, and possible dopant depletion effects. A new mask set with test structures specifically characterizing these issues was designed, and samples were fabricated with this mask set. Measurements are in progress.

Once the questions related to $WSi_2$/Si contacts are answered, we will be ready to begin transient process characterization experiments. For our initial

experiments we have decided to look at the annealing of relatively low dose implants. These are often used for threshold voltage control in MOS transistors. The experiments were designed to look at three phenomena. The first is the electrical activation of the implanted species. In addition to that we are concerned with the annealing of damage created by the implant. Finally, since these implants are typically done through the thin gate oxide, we are concerned with the effect of oxygen knock-ons. The devices for these experiments are included in the mask set being used for the $WSi_2$/Si contact study.

In conclusion, during the last six months we have finished the tests on MOS capacitors using $WSi_2$ gates, have begun the tests on $WSi_2$/Si contacts and have started planning the first experiments which will utilize this technology for characterization of transient process kinetics.

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## CHEMICAL VAPOR DEPOSITION OF SILICON

K. C. Saraswat, M. M. Mandurah and T. I. Kamins

### A. Polycrystalline Silicon

Polycrystalline silicon is generally viewed as composed of small crystallites joined together by grain boundaries. Inside each crystallite, the atoms are arranged in a periodic manner forming small single crystals,

while the grain boundaries are composed of disordered atoms with incomplete bonding. The high concentration of defects and dangling bonds at the grain boundaries cause trapping states capable of immobilizing both dopant atoms and charge carriers, thus reducing the number of free carriers available for conduction. Furthermore, because of the disordered nature of the grain boundaries, the carriers suffer additional reflection at the grain boundaries resulting in reduction of mobility. In this work a new model has been developed, which shows that electrical conduction in polycrystalline silicon is controlled by the combined mechanisms of dopant segregation, carrier trapping, and carrier reflection at the grain boundaries.

1. Dopant Segregation

In our previous work we have studied the segregation of arsenic to the grain boundaries of polycrystalline silicon [10,11]. In this work, studies on segregation of phosphorus and boron are being reported.

Dopant segregation to the grain boundaries can be modeled by [10,11]

$$\ln \frac{N_{GB}}{N_G} = \ln \frac{A \cdot Q_s}{N_{Si}} + \frac{Q}{kT_A} \tag{14}$$

where $A = \exp(-S/k)$ and $N_G$ and $N_{GB}$ are the dopant concentrations/cm$^3$ in the grains and at the grain boundaries, respectively, $Q_s$ is the density of grain boundary sites/cm$^3$, $N_{Si}$ is the number of Si atoms/cm$^3$, Q is the heat of segregation, S is the vibrational entropy, $T_A$ is the anneal temperature, and k is the Boltzmann's constant. In order to determine the segregation parameters of Eq. (14) poly-Si films of 0.5 μm thickness were ion implanted with P or B and first annealed at 1000 or 1100°C for one hour to activate and redistribute the dopant atoms and to stabilize the grain size so that further, lower temperature, annealing would not change the grain size appreciably. After the initial anneal, some of the samples were further annealed at lower

temperatures for times long enough for all resistivity changes to reach saturation. Resistivity, mobility and carrier concentration were measured by fabricating ring and dot structure resistors and van der Pauw structures. The experimental details are similar to Ref. [10,11]. From these measurements values of $N_G$ and $N_{GB}$ were calculated.

Fig. 16 shows plots of $\ln(N_{GB}/N_G)$ vs. $1/T_A$ for poly-Si films doped with phosphorus. For comparison the data for arsenic obtained from our previous studies is also included in Fig. 16. In both cases a linear dependence on $1/T_A$ was obtained for each curve; the slope of the lines gives the heat of segregation. Table 1 shows values for the heat of segregation, Q and $A \cdot Q_s/N_{Si}$, for the two dopants. No changes in carrier concentration were observed in the case of boron as shown in Fig. 17, indicating that there is no appreciable segregation of boron into the grain boundaries.

Table I

| $N_d$ | Q | $AQ_s/N_{Si}$ | A |
|---|---|---|---|
| Arsenic $2 \times 10^{19}$ $cm^{-3}$ | 10.1 Kcal/mole | .049 | 3.02 |
| Arsenic $6 \times 10^{19}$ $cm^{-3}$ | 9.58 Kcal/mole | .036 | 2.67 |
| Phosphorus $2 \times 10^{19}$ $cm^{-3}$ | 10.2 Kcal/mole | .040 | 2.46 |

2. Electrical Conduction in Polycrystalline Silicon

After accounting for the fraction of the dopant atoms segregating to the grain boundaries, the remaining dopant atcms are distributed uniformly within the grains. The number of ionized dopant atoms are distributed uniformly within the grains. The number of ionized dopant atoms in the grains

can be determined using the Fermi-Dirac statistics in a similar way as in single-crystal silicon. Some of the resulting carriers are trapped at the grain boundaries, thus further reducing the number of free carriers available for electrical conduction. As a consequence of carrier trapping, a portion of each grain is depleted, creating potential energy barriers, $qV_b$, which impede the motion of carriers from one crystallite to another. Charge transfer in this case, is controlled by thermionic emission over these barriers which have a maximum height given by

$$qV_b = q^2Q_t^2/8\ \epsilon N_G \qquad (15)$$

where $Q_t$ is the density of trapping states/cm$^2$ at the grain boundary [12].

Due to the highly disordered nature of the grain boundaries, the material at the grain boundaries behaves as an intrinsic wide-band-gap semiconductor, resulting in the formation of a heterojunction at the interface between a crystallite and a grain boundary. Therefore, as shown in Fig. 18, the effect of the grain boundaries can be modeled by potential barriers, the height of which, $q\phi_{gb}$, relative to Fermi level, is equal to $E_{gb}/2$, where $E_{gb}$ is the band gap of the grain-boundary material, and the width of each of these potential barriers, $W_{gb}$, is approximately equal to the width of the grain boundary. Thus, in order to move from one crystallite to another, the carriers have to either tunnel through a grain boundary barrier or be sufficiently energetic to be thermally emitted over the barrier [13].

By combining the mechanisms of dopant segregation, carrier trapping, and carrier tunneling, the following current-voltage relationship in polycrystalline silicon can be obtained

$$J = q\left(\frac{4\pi m^* k^2 T^2}{h^3}\right) \times \exp\left(-\frac{\xi}{kT}\right) \times \frac{\exp(-b_1)}{(1-c_1 kT)} \times$$

$$\exp\left(-\frac{qV_b}{kT}\right) \times 2 \sinh\left[\frac{1 + c_1 kT \frac{N_G W_{gb}}{Q_t}}{1 + \frac{N_G W_{gb}}{Q_t}} \times 2\frac{qV_o}{kT}\right] \quad (16)$$

where $V_o$ is the total voltage across the grain boundary, $\xi = E_c - E_F$ and $b_1$ and $c_1$ are given by

$$b_1 = \frac{4\pi W_{gb}}{h} (2m^*)^{1/2} (q\phi - qV_b)^{1/2} \quad (17)$$

$$c_1 = \frac{2\pi W_{gb}}{h} (2m^*)^{1/2} (q\phi - qV_b)^{-1/2} \quad (18)$$

where $q\phi = q\phi_{gb} - \xi$.

This current voltage relationship shows that the electrical properties of polycrystalline silicon are a function of the grain-boundary properties (the density of segregation sites at the grain boundary, $Q_s$, the density of carrier trapping states, $Q_t$, and the height and width of the grain boundaries, $\phi_{gb}$ and $W_{gb}$ respectively).

The grain-boundary properties have been shown to be a function of both the type of the dopant and high-temperature processing cycles applied to the films. Thus, by accounting for all of the above effects, this model can also predict the electrical properties of polycrystalline silicon as a function of high temperature processing.

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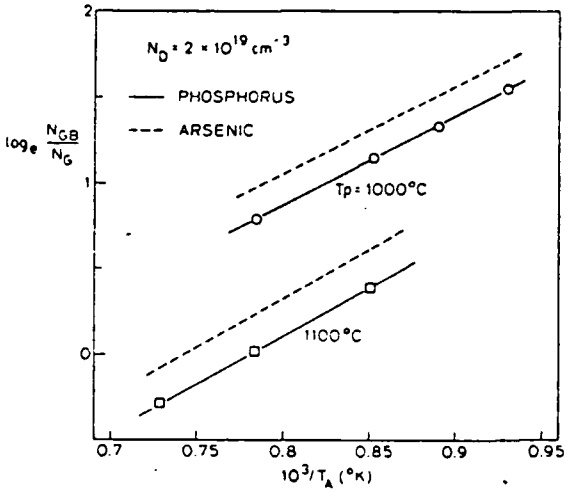


Fig. 16: $N_{GB}/N_G$ as a function of final annealing temperature for average P or As concentration of $2 \times 10^{19}\ cm^{-3}$ and pre anneal temperatures of 1000 and 1100°C.

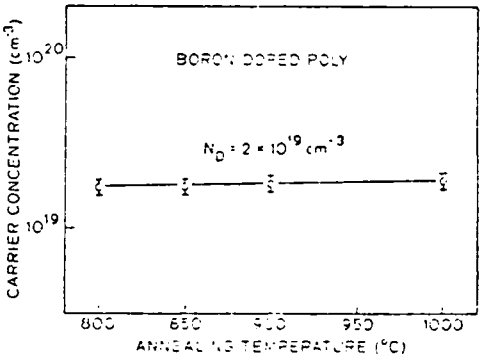


Fig. 17: Carrier concentration vs. annealing temperature for boron doped poly-silicon.

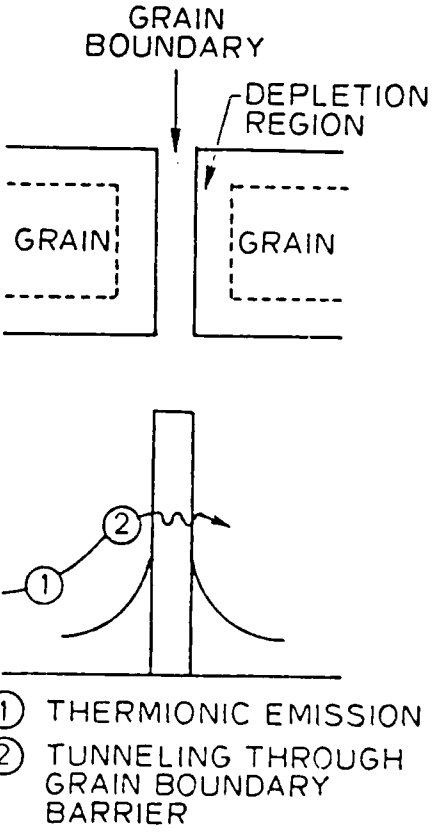


Fig. 18: Schematic representation of a carrier transport across a grain boundary: (1) Thermionic emission over the barrier caused by carrier trapping, (2) Tunneling through the grain boundary barrier.

B. Refractory Metal Silicides

(K. Saraswat, F. Mohammadi)

1. $WSi_2$ Gate MOSFETs

Use of $WSi_2$ as gate electrode and interconnection material in MOS integrated circuits has been proposed because of its higher conductivity compared to doped polycrystalline silicon [14-19]. Two techniques have been proposed for this application. In one technique doped polycrystalline silicon is first deposited on gate oxide and then a layer of $WSi_2$ is deposited on top of it [14-19]. Thus the MOS properties are similar to the conventional silicon gate MOS technology. In the second technique used in this work, $WSi_2$ is directly deposited on $SiO_2$ and is used as the gate material [15-18]. Feasibility of the use of $WSi_2$ as gate electrode has been demonstrated by fabricating MOS capacitors [16-18]. The capacitors showed good MOS properties, i.e., low values of fast surface-state and fixed interface charge densities. In this work enhancement- and depletion-mode NMOS transistors for an inverter have been fabricated.

For a nominal supply voltage of $V_{DD}$ = 5 V, $x_o$ = 750 Å, $V_{Td}$ = -3 V, $V_{Te}$ = 1 V, fabrication process for an NMOS inverter was simulated, using the SUPREM program [20], for the given values of threshold voltages and $Q_{ss} = 7 \times 10^{10}$ $cm^{-2}$, where $V_{Td}$ and $V_{Te}$ are threshold voltages of depletion-mode and enhancement-mode transistors, respectively. The value of the work function of $WSi_2$ is higher than that of aluminum or $n^+$ poly-Si gate electrodes [18], therefore, the process was accordingly modified to obtain required threshold voltages and proper characteristics of the MOS transistors.

The devices were fabricated on (100) boron-doped 2 to 4 Ω-cm silicon wafers, and Fig. 19 summarizes the process. A channel-stop implant of boron with a $0.5 \times 10^{13}$ $cm^{-2}$ dose at 160 keV prevented leakage between the adjacent

devices. Field oxide of 7000 Å was used for device isolation, and was grown via an isoplanar process [21].

A boron gate-threshold-control implant was performed at a dose of $1.5 \times 10^{11}$ $cm^{-2}$ and energy of 35 keV, followed by a second deep boron implant with a $3 \times 10^{11}$ $cm^{-2}$ dose at 100 keV to control bulk punchthrough, and Tungsten silicide of 2500 Å thickness was RF sputtered from a hot-pressed alloy target of stoichiometric composition. Pattern definition was acheived by means of a chemical etch of $WSi_2$ in a $HNO_3$:$NH_4F$ solution (volume ratio of 50:1). The etch rate of $WSi_2$ was 450 Å/min. An arsenic source-drain implant was performed with a $6 \times 10^{15}$ $cm^{-2}$ dose at 100 keV. A thin layer of thermal oxide was grown to cover the source and drain so as to minimize leakage current and to prevent the out-diffusion of arsenic. A pyrolytically deposited $SiO_2$ + $P_2O_5$ (p-glass) layer of 6000 Å was deposited and contact vias were opened, followed by p-glass reflow at 1000°C in $N_2$. Aluminum+2% silicon was then evaporated and defined, followed by a forming-gas anneal at 450°C to improve the surface states. The devices were tested and transistor parameters were measured.

Fig. 20 shows the characteristics of a typical pair of MOS transistors. The locations of the saturation regions of the enhancement-mode (20a) and depletion-mode (20b) transistors differ because of the difference in their threshold voltages. From the measurements on the test structures, the mobile charge density was found to be negligible. The densities of the fixed interface charge and fast surface states were measured to be $7 \times 10^{10}$ $cm^{-2}$ and $1.5 \times 10^{10}$ $cm^{-2}$ $eV^{-1}$, respectively. The dielectric breakdown strength of the gate oxide was found to be nominally about 8 MV/cm. $V_{Te}$ and $V_{Td}$ were measured to be 1.2 and -2.8, respectively, for $x_o$ = 750 Å, and these values are in less than 10 percent deviation from estimated threshold voltages.

Measured saturation electron mobilities of 210 $cm^2/v$ sec at $V_D$ = 7 V for the depletion-mode devices were found to be consistent with the electron mobility of $MoSi_2$ gate transistors [22]. The sheet resistances of $WSi_2$ and diffusion regions were 6 and 30 Ω/□, respectively, and the drain and source junction depth was 0.3 μm. In the enhancement-mode transistor, the drain-source breakdown voltage was 25 V.

In conclusion, a process to fabricate an invertor with $WSi_2$ gate NMOS transistors has been designed and the resulting enhancement and depletion-mode transistors have been characterized. Because of improved conductivity of material its use as a gate and interconnecting material is recommended.

Table 2

MEASURED DATA OF ENHANCEMENT- AND DEPLETION-MODE MOS TRANSISTORS

| | Enhancement Mode | Depletion Mode |
|---|---|---|
| Surface doping concentration under gate ($cm^{-3}$) | Boron, $10^{16}$ | Phosphorus, $6 \times 10^{16}$ |
| Channel length x width (μm x μm) | 5 x 10 | 10 x 5 |
| Threshold Voltage (V) | 1.2 | -2.8 |
| Transconductance at saturation ($\nu$) | $1.35 \times 10^{-4}$ | $1.75 \times 10^{-5}$ |
| Electron mobility of channel at saturation ($cm^2/v$ sec) | 210 | 110 |

2. Thermal Oxidation of Silicides of Mo and Ta

We have studied the properties of $WSi_2$ up to now in this program. From now onwards, we will also be studying the properties of the other silicides

and will compare them to $WSi_2$. Initially $MoSi_2$ and $TaSi_2$ have been chosen. Their deposition by the technique of cosputtering is being done. The effect of annealing on resistivity is being studied. Work has been started to study the thermal oxidation of $MoSi_2$ and $TaSi_2$. Initially oxidations have been performed in dry oxygen. The $TaSi_2$ films showed anomalous oxidation behavior, while, the $MoSi_2$ films showed good oxidation behavior, similar to $WSi_2$ films. Detailed analysis of these films is being done by Auger sputter profiling.

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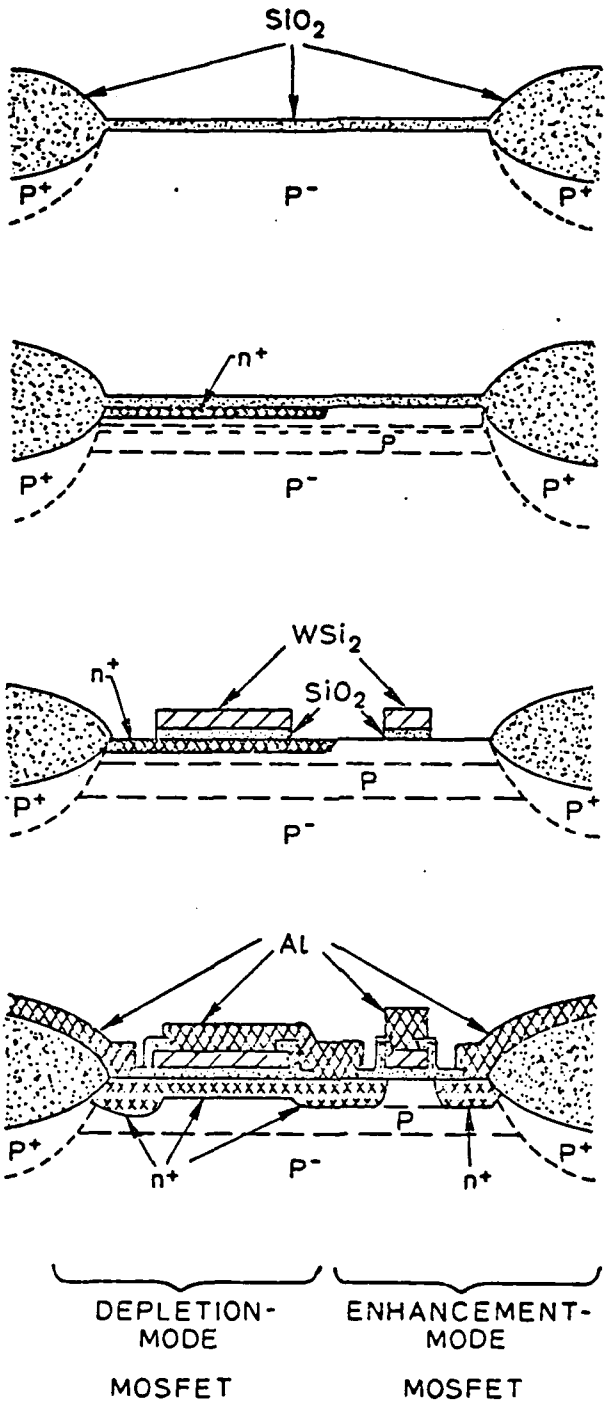
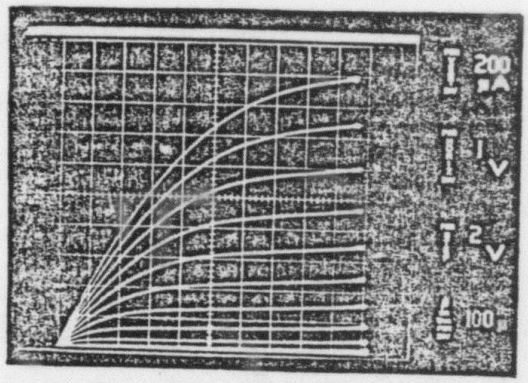
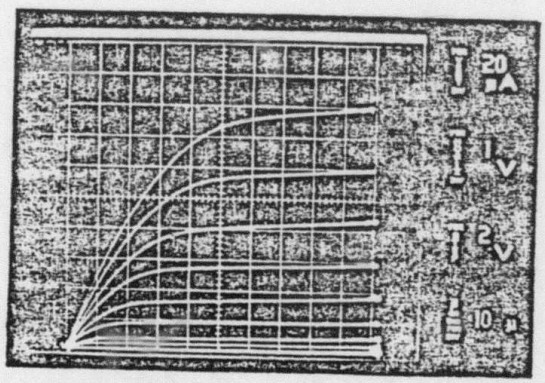



Fig. 19: Fabrication sequence of the Enhancement- and depletion-mode NMOS transistors.




(a)




(b)

Fig. 20: Drain Current vs. drain-source voltage characteristics.

A. Enhancement-mode transistor (L = 5 μm w = 10 μm).

B. Depletion-mode transistor (L = 10 μm w - 5 μm).

## MATERIALS ANALYSIS/INTERFACE PHYSICS

R. W. Barton, J. W. Rouse, C. R. Helms, B. E. Deal, R. Razouk

### A. Introduction

In this period we have concentrated on modeling of impurity redistribution during oxidation particularly related to segregation effects at the Si-$SiO_2$ Interface.

Interface segregation, an important phenomenon in fields such as metallurgy and heterogenous catalysis, is becoming increasingly important in the study of thin films. In its more familiar context, segregation has been used to explain temper embrittlement in metal alloys as well as the activity of heterogeneous alloy catalysts [21]. Segregation is in fact expected when a multi-component system reaches equilibrium at the interface between two bulk phases [22]. Since one component will generally have a lower free energy in the interface region, that component will preferentially segregate to that region. In semiconductors, however, where the distribution of dopants and other impurities is an important determinant of device behavior, segregation effects have only recently been considered [23,24]. These effects are expected to become increasingly important as device dimensions decrease.

We have used Auger sputter profiling to measure the distribution of phosphorus and chlorine at the Si-$SiO_2$ interface [23]. We find that both impurities tend to segregate to the interface. The significance of this observation for the case of phosphorus, an n type dopant in silicon, is illustrated in Fig. 21. The distribution has been expected to be influenced by oxidation: phosphorus is piled-up in front of the moving interface because it is less soluble in $SiO_2$ than it is in silicon. However, because phosphorus is a relatively fast diffuser, this pile-up is expected to extend for at least a micron into the silicon, and to be no more than 1.1 times more

concentrated at the interface than in the bulk [25]. This contrasts with our Auger sputter profiles, which reveal large concentrations (up to ten times the bulk level) occurring within a 50 Å region at the $Si/SiO_2$ interface.

Further studies have revealed that this pile-up near the interface is an interface segregation effect which occurs in addition to the "normal redistribution" of phosphorus, and is not associated with the actual movement of the $Si/SiO_2$ interface. For instance, the concentration of phosphorus increases during early oxidation times - at a rate that cannot be accounted for by mere redistribution from the $SiO_2$. Furthermore, if a thin ( <100 Å ) oxide is annealed, the interface concentration will increase further until it reaches a maximum or "saturated" level, characteristic of measurements on thicker oxides. Longer oxidations or post-oxidation anneals do not alter the saturated distribution. The phosphorus is therefore thought to be segregated, or attracted, to the interface by a lower chemical potential in that region.

Large amounts of phosphorus can exist in the saturated pile-up, up to $7 \times 10^{14}$ atoms per square centimeter. Further models of dopant distribution should account for this segregation, and include its dependence on processing parameters such as oxidation time, temperature, and bulk doping level. Similarly large amounts of chlorine, an additive in the oxidation ambient, are found at the $Si-SiO_2$ interface (see Fig. 22).

Past studies of chlorine distributions in $SiO_2$ grown in $O_2/HCl$ mixtures [26-29] showed high levels of chlorine residing in the oxide near the interface with much lower levels of chlorine in the bulk oxide. These results have been compiled largely from SIMS and RBS data, and show the FWHM of the chlorine pile-up to be typically 150-200 Å. The total chlorine incorporated in this region has been seen to increase with oxide growth temperature, oxide thickness, and partial pressure of HCl in the ambient. ELectron microscopy studies [30] have also provided evidence that this chlorine resides near the

interface in a laterally inhomogeneous phase. However, while these studies have provided a good measure of the degree of chlorine incorporation, problems of depth resolution and broadening [31] intrinsic to the RBS and SIMS techniques make it difficult to carefully determine the actual width and peak positions of these chlorine distributions. The RBS depth resolution reported by van der Muelen et al. [28] was 200 Å. Sputtering ion energies in the SIMS work ranged from 6 to 8 keV leading to knock-on broadening of approximately 90 - 120 Å [31]. These considerations make clear the difficulty in carefully determining the actual width and peak positions of these chlorine distributions.

B. Experimental

Our chemical concentration profiles are obtained by Auger sputter profiling with a Varian 2730 Auger Spectrometer. Profiles are obtained by monitoring the heights of characteristic Auger spectra while simultaneously sputtering with a neon ion beam. Several experimental factors must be considered before these profiles are quantitatively interpreted in terms of chemical concentration and interface width.

Concentrations are generally determined by comparing the peak to peak heights of the Auger derivative spectra. The phosphorus LVV spectrum, for instance, is compared in height to the LVV spectrum of the silicon substrate. These ratios must be corrected by a spectral sensitivity factor, determined from calibrated standards. We use Si or $SiO_2$ samples ion implanted with a known dose of impurity as our standard. Care is taken to insure that the incident electron current is low enough to prevent effects such as desporption, decomposition, and diffusion in the sample. Typically we use 4.5 keV electrons at currents of 10 microamps, rastered over a 600 micron square area. We find our concentration measurements to be reproducible to ±10%.

Our depth scale is determined by the sputter rate, which is measured by the time taken in sputtering through an $SiO_2$ film of known thickness. The sputter rates in Si and $SiO_2$ are not expected to be different by more than 5 or 10 percent. The depth resolution is determined to a certain extent by the electron escape depth, but primarily, by the mixing effect of the sputter ion beam. In previous work, we have measured how profiles are broadened by sputter ions of different mass, energy, and incidence angle [31]; neon, for instance, at a sputtering energy of 1 keV, will broaden the profile as much as 30 Å.

Several chemical concentration profiles, such as shown in Fig. 22, were obtained by the above methods. Phosphorus concentrations as high as $1.2 \times 10^{21}$ $cm^{-3}$ have been measured in the interface of samples doped in the bulk at concentrations of $1.2 \times 10^{20}$ $cm^{-3}$. Chlorine peak concentrations as high as $3 \times 10^{20}$ $cm^{-3}$ have also been measured. Both pile-ups are typically 40 Å in width, with a relative displacement that associates the phosphorus primarily with the silicon side of the interface and chlorine with the $SiO_2$ side.

Since our profiles are significantly broadened by the mixing of the ion beam, the actual profile may actually be quite a bit narrower and proportionately more concentrated than shown. The integrated concentration is expected to be an accurate indication of the amount of impurity at the interface. Typical values for phosphorus are $7.0 \times 10^{14}$ $cm^{-3}$, measured after an 800° oxidation, which, if concentrated in one atomic layer at the interface, would comprise 50% of that layer.

C. Clorine Segregation at the $Si-SiO_2$ Interface During Oxidation in $O_2$/HCl Mixtures

Our own ASP studies on $O_2$/HCl grown oxides may be summarized as follows: (1) High levels of chlorine (up to $2 \times 10^{15}$ $cm^{-2}$) reside in the oxide near the interface in a region less than 50 Å wide, in contrast to the results of

SIMS and RBS studies. The bulk oxide chlorine levels are much lower, $<1 \times 10^{19}$ $cm^{-3}$; (2) The total interface chlorine increases with temperature for a fixed oxide thickness; (3) The total interface chlorine for a fixed temperature increases monotonically with oxide thickness. We believe the evolution of the chlorine distribution can be described in terms of a diffusion process of a chlorine species ot the $SiO_2$/Si interface region where it is incorporated into the near interface $SiO_2$. With the arrival of sufficient chlorine, a new phase is nucleated which eventually grows and coalesces to form blisters at the interface.

The samples in this study were (100) and (111) oriented n-type silicon oxidized in $O_2$/5% HCl at 1000°C and 1100"C. All samples were examined using Auger sputter profiling. We also profiled oxides grown in $O_2$ with no HCL as controls. To calibrate Auger chlorine signals we grew $SiO_2$ at 1000°C to approximately 1000 Å and then implanted these with $^{35}Cl^+$ at 50 keV for a total dose of $3.0 \times 10^{15}$ $cm^{-2}$.

Work by Chou, Osburn, van der Meulen, and Hammer [32] shows that the Auger technique mobilizes chlorine in $SiO_2$ and causes it to desorb. We have completed extensive studies [33] enabling us to quantify and minimize these effects. We have determined that electron beam irradiation has contributed less than $1.4 \times 10^{13}$ $cm^{-2}$ to the interface chlorine in our data, and is therefore clearly not a dominant factor.

All of the $HCl/O_2$ grown samples are characterized by bulk oxide chlorine levels below our detection limit of $1 \times 10^{19}$ $cm^{-3}$, and chlorine peaks on the oxide side of the interface about 10 Å from the oxygen 50% point. In contrast to earlier work [26-29] the chlorine peaks had a FWHM of 30-50 Å. These widths are upper limits. Taking broadening factors into account, we would describe the actual peak widths as 30 Å or less, and the interface chlorine could

conceivably occupy only a few monolayers in the interface region. To determine the effects of growth time and temperature on chlorine incorporation, we integrated the chlorine profiles to determine the total amount of chlorine in the interface region. We found that chlorine incorporation increases with oxidation temperature and oxide thickness. Data are plotted in Fig. 23 for total interface chlorine versus oxide thickness for our samples.

To model the chlorine incorporation process we have used a steady state approximation to chlorine into the interface region (treated as a chlorine sink) by a reaction rate constant. By equating bulk and interface fluxes and integrating the interface flux overtime, we obtain an expression for the total interface chlorine given by

$$Q = Q_o + \frac{P}{B/A}\left(\frac{x_o - x_i}{A/2}\right) + \left(1 - \frac{\lambda}{A/2}\right) \ln\left(\frac{x_o + \lambda}{x_i + \lambda}\right) \qquad (19)$$

$Q_o$ is some initial Q at $x = x_i$; B, A and $x_i$ are the Deal-Grove oxide growth parameters. P is a permeability for Cl in $SiO_2$ which can be related to the diffusion coefficient and surface concentration of the chlorine as well as any field present; $\lambda$ is related to the ratio of the diffusion coefficient to reaction rate constant. The three curves in each case represent different limits for the parameter $\lambda$. From the data we cannot determine $\lambda$ except to the extent that the case $\lambda \to \infty$ is inconsistent with the data. Using the model for a given $\lambda$ however, we can predict the total interface chlorine for a given oxide thickness.

## D. Segregation Modeling for Phosphorus at the Si-$SiO_2$ Interface

Impurities will segregate to an interface when they have a lower chemical potential in that region. Several physical mechanisms might be used to account for this effect: charged impurities will be attracted if they can reduce their

electronic energy. All of these cases, however, can be treated thermodynamically in a simple way by assuming that the impurity is held at the interface in a separate chemical phase with a lower standard state free energy. In the limit of low concentration, its profile will be determined by a Boltzmann relation such as:

$$C_I = C_B \exp(-\Delta\mu^\circ/kT) \qquad (20)$$

where $\Delta\mu^\circ$ represents the chemical potential difference between bulk and interface and includes both the heat and entropy of segregation.

This relationship has in fact been verified in our Auger sputter profiles of phosphorus samples that had been post-oxidation annealed at a series of different temperatures. We find a reversible dependence of phosphorus interface concentration on temperature: The lower temperatures being associated with higher concentrations at the interface. The width of the profiles is not significantly affected by temperature. Fig. 24 shows the expected temperature dependence as an Arhenius plot, verifying again that the phosphorus distributes itself in equilibrium with the interface. The slope of the graph indicates that the heat of phosphorus segregation, Q is 0.26 electron volts.

As indicated previously, in early oxidation times the segregated layer is observed to increase in concentration at a rate faster than that expected by redistribution from the $SiO_2$. Before the interface reaches its saturated or equilibrium concentration it presumably fills with phosphorus by diffusion out of the bulk of the silicon as well as the $SiO_2$. We have modeled this diffusion process by assuming that the interface represents initially a square well in the chemical potential of phosphorus.

The model then uses common values of phosphorus diffusion coefficient and $Si/SiO_2$ interface velocity to predict the amount of time necessary to fill this well to its saturated value. Our diffusion model accurately predicts the relationship between total interface concentration and oxidation time. It also

determines phosphorus concentrations in the silicon near the interface. Fig. 25 compares the prediction of the diffusion model to an actual Auger sputter profile.

Because our Auger sputter profiles are broadened by the mixing effect of the ion beam, our knowledge of the relative depth and width of the potential well remains incomplete. We find that adjustment of these parameters in our diffusion model has no significant effect on its results, their being dependent only on the total volume of the potential well. The Arhenius plot of Fig. 24 is useful because it defines a heat of segregation, but the depth of the chemical potential well also depends on an as yet undetermined entropy of segregation. Nevertheless, we have shown that knowledge of the amount of phosphorus in a segregated layer saturated at one oxidation temperature is sufficient to predict the amount that will appear there after other oxidation time and temperatures.

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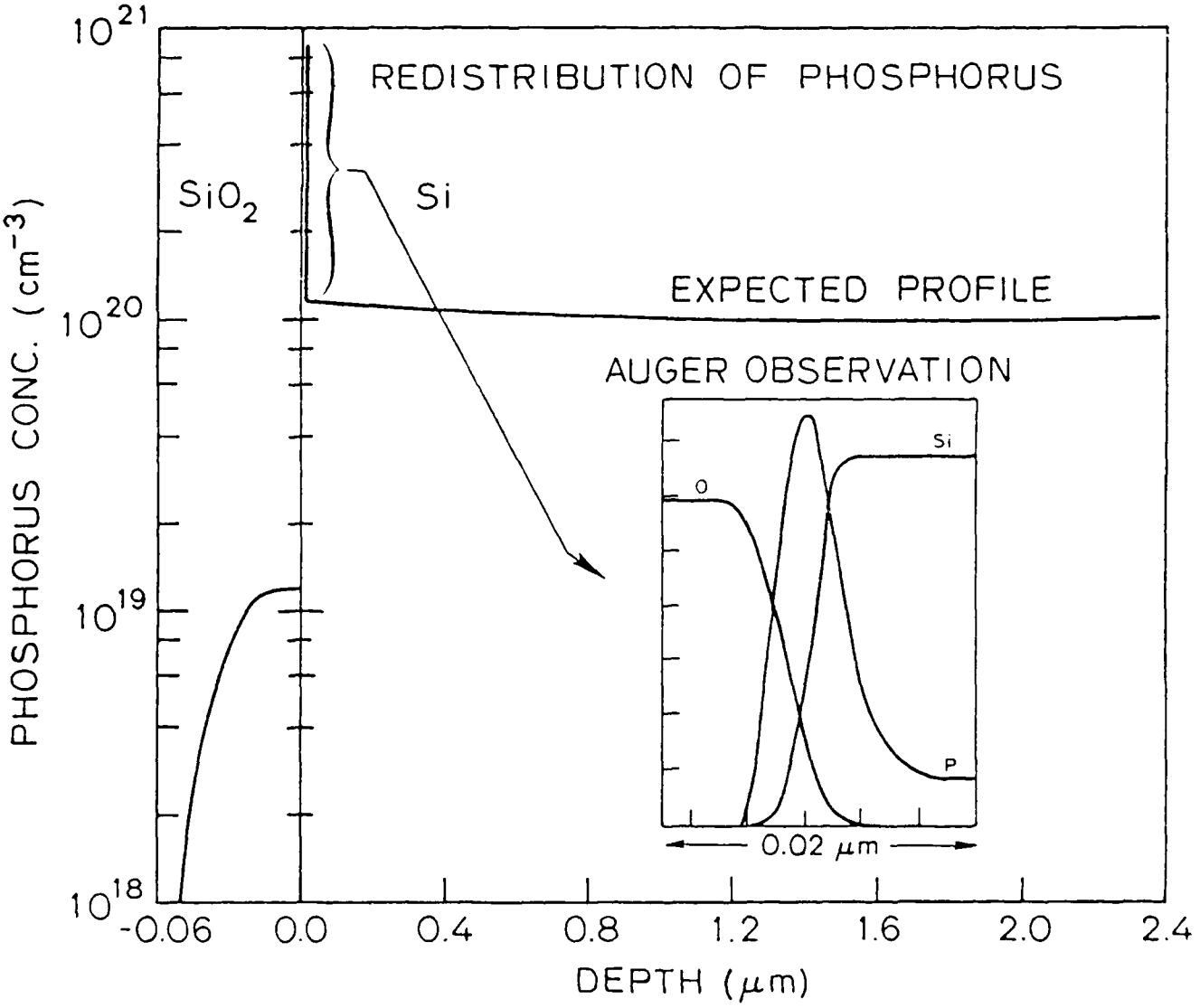


Fig. 21. A comparison of phosphorus distributions near a moving $Si/SiO_2$ interface. The "expected" profile results from bulk diffusion calculations, the narrow peak at the interface represents the results of Auger sputter profiling.

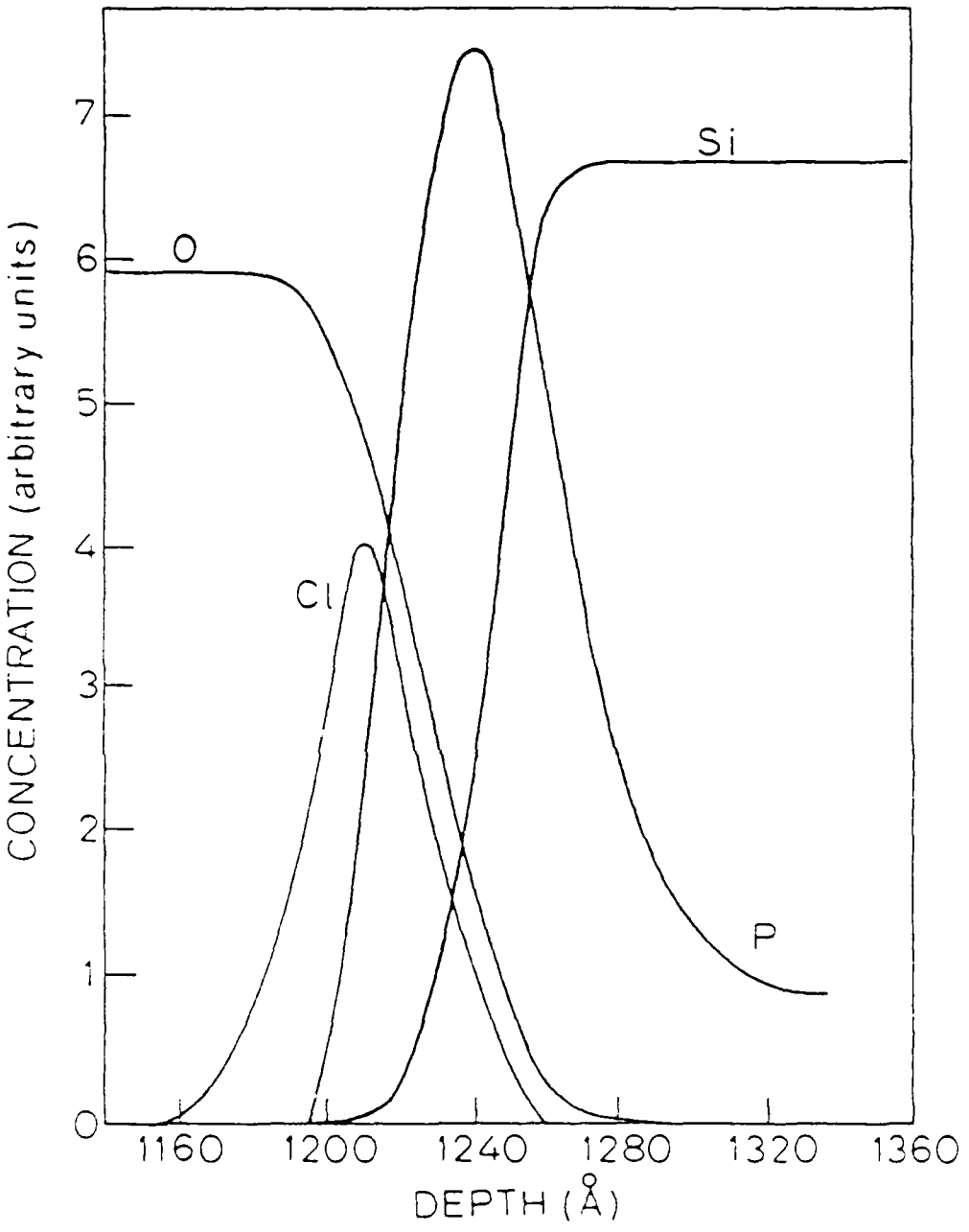


Fig. 22. Auger sputter profiles of oxygen "free" silicon, phosphorus, and chlorine in the region of the $Si/SiO_2$ interface. $SiO_2$ is on the left, Si on the right. The depth scale originates on the surface of $SiO_2$.

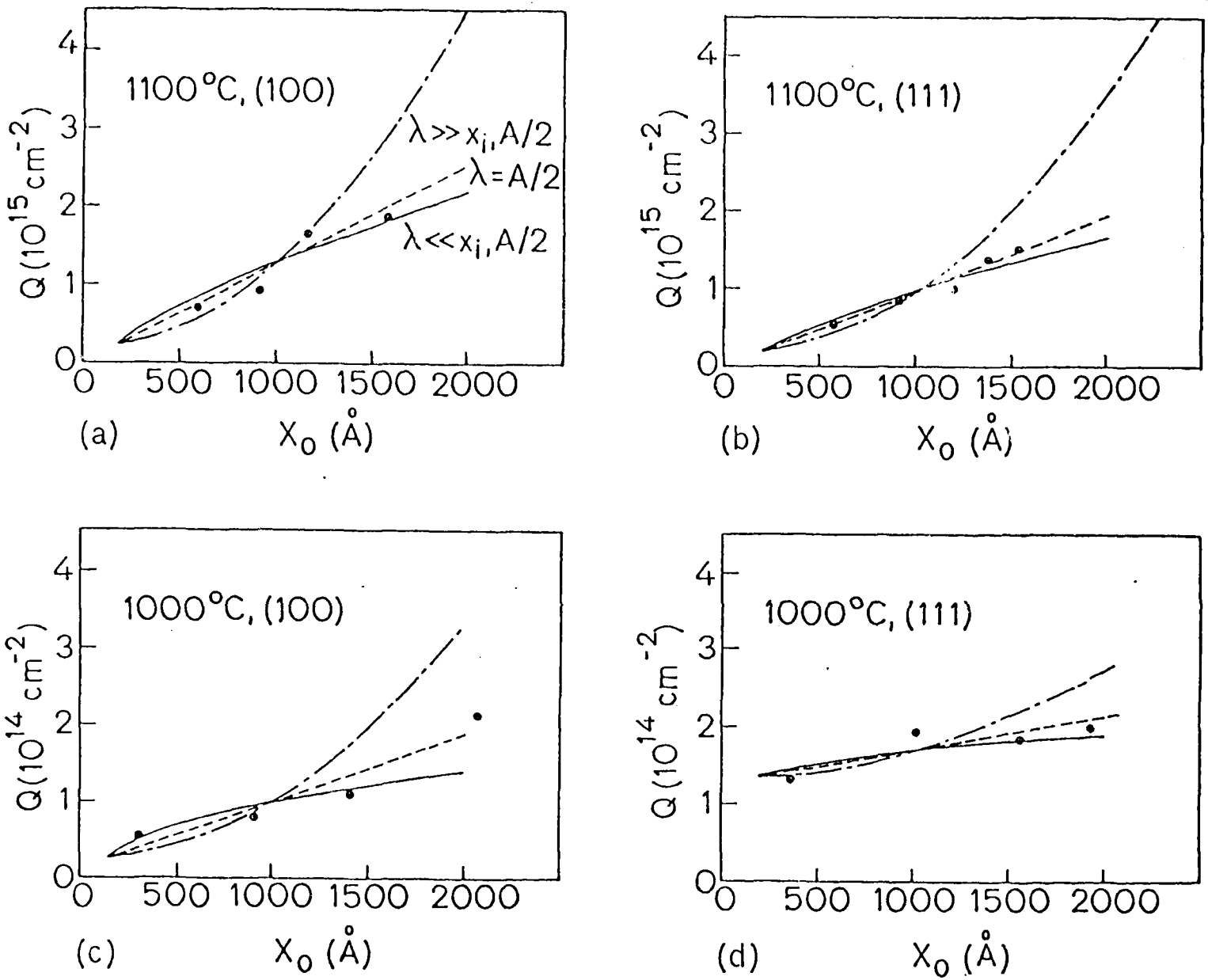


Fig. 23. Shows total interface chlorine Q vs. oxide thickness $x_o$ for oxides grown in $O_2$/5% HCl at 1100°C, 1000°C on (100), (111) substrates. Note the scale change for Q. Units are $10^{15}$ $cm^{-2}$ for 1100°C samples and $10^{14}$ $cm^{-2}$ for 1000°C samples.

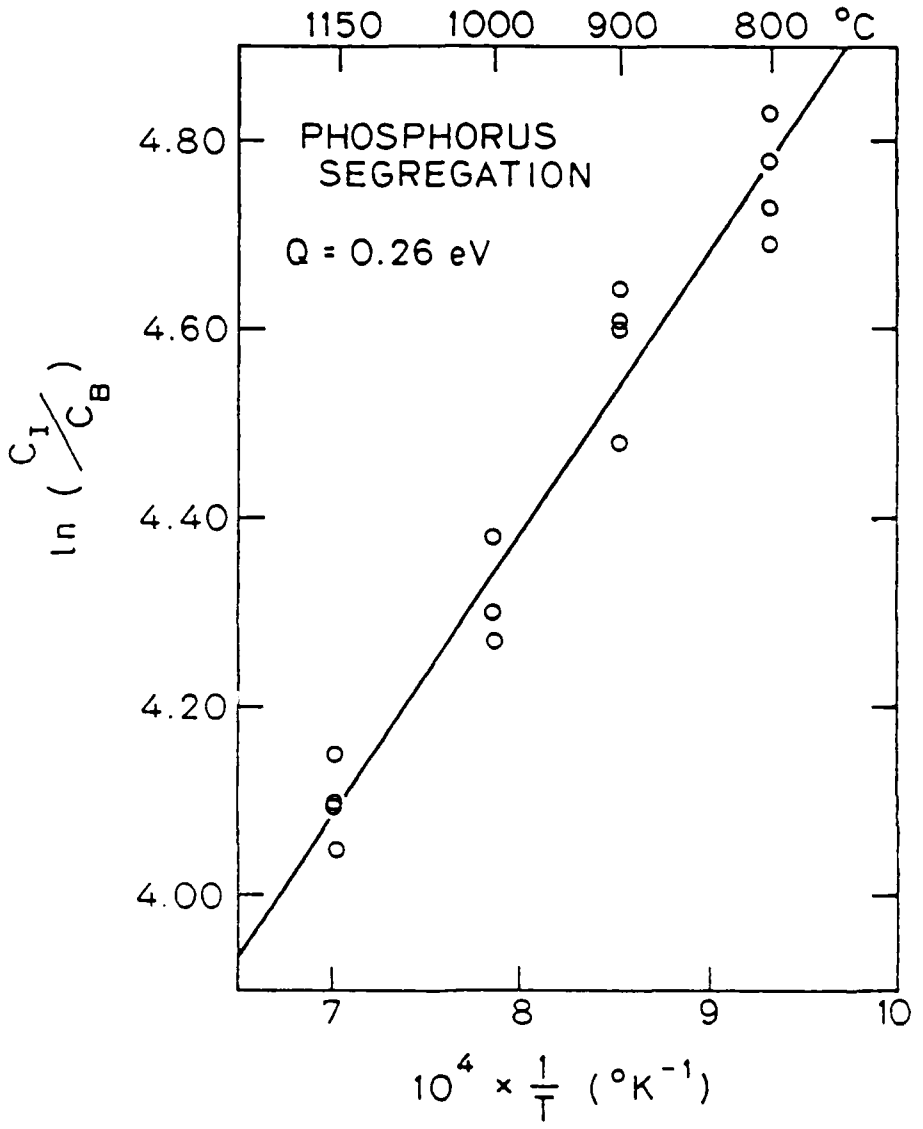


Fig. 24. The temperature dependence of phosphorus interface segregation. The interface concentrations are determined by integrating the Auger sputter profile and assuming that the excess phosphorus concentration resides in a single atomic layer at the interface.

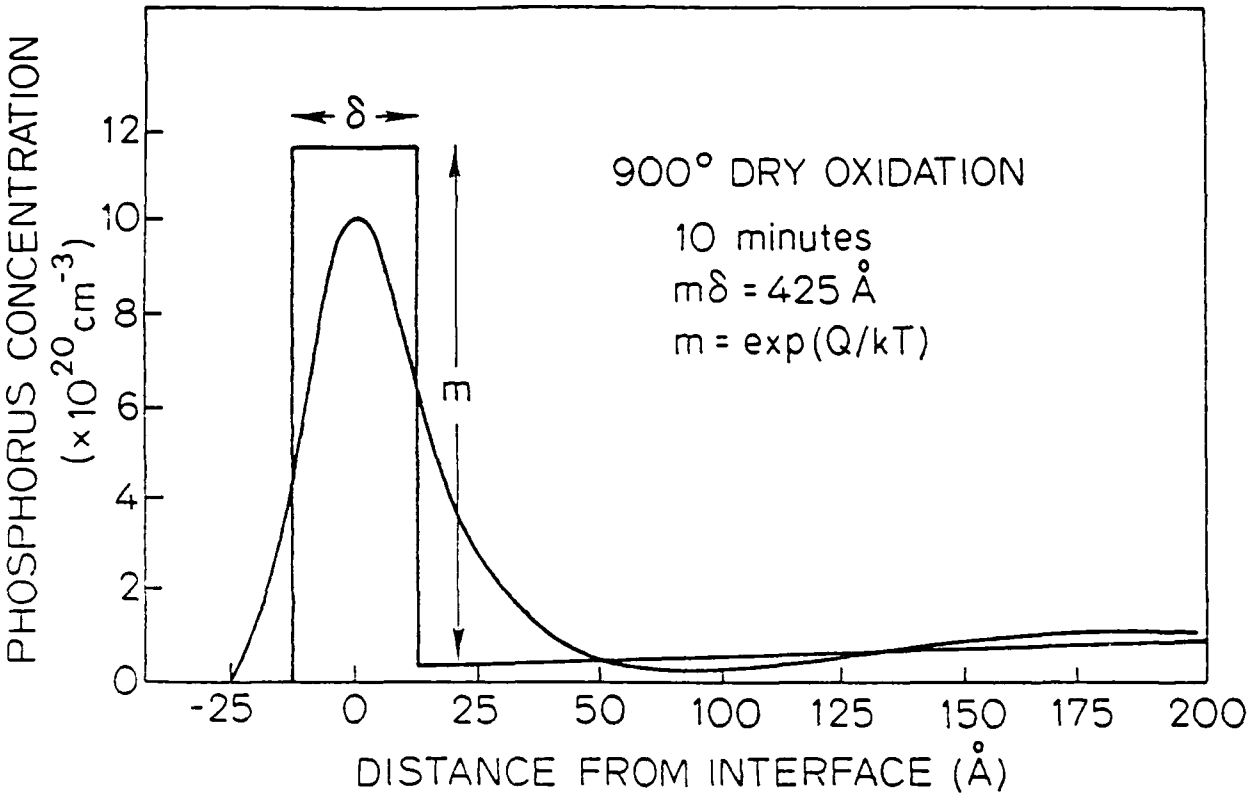


Fig. 25. A comparison between diffusion theory and experiment for an as yet "unsaturated" phosphorus profile that had been oxidized at 900°C for ten minutes. The theory predicts the area under the profile as well as the depletion in the silicon that accompanies diffusion from the bulk.

# COMPLETE PROCESS AND DEVICE SIMULATION

R. W. Dutton, S. Chen, K. Doganis, S. Hansen,
H. G. Lee, L. Mei, S. Y. Oh, B. Swaminathan

## A. Introduction

During this contract period there have been a number of advances in the overall process modeling capabilities of SUPREM. A current theme of program development is to generate a multilayer analysis capability. In particular, the multilayers of polycrystalline impurity diffusion sources for buried contacts and polycrystalline MOSFET gate layers with associated oxide layers at both interfaces are two examples of major importance for device applications. The framework for a multilayer process simulator, SUPREM III was defined during the contract period. In addition, experiments and simulations involving multilayer polycrystalline structures were pursued. Section I presents details of the efforts in characterizing and modeling multilayer poly structures. Section II gives a summary of the definition and implementation status of SUPREM III.

Over this contract period there have been extensive interactions with other research groups involved in process modeling. Moreover, the release of both one- and two-dimensional device analysis programs developed under the previous contract has helped to clarify the overall objective of this period -- to couple process modeling information directly with device analysis and circuit design. Section III gives a summary of interactions with industry and other research groups concerning process modeling. Finally, in Section IV the status of device analysis capabilities as they relate to SUPREM are summarized.

B. Experiment and Modeling of Multilayer Polycrystalline Silicon

Multilayer structures in the design of integrated circuits are rapidly becoming a requirement for the increased circuit density. Typical multilayer structures involve different materials such as metal, polycrystalline silicon, insulating layers, silicide, etc. Clearly the performance of each layer as well as the structure as a whole depends critically on the process conditions. While most of the simulators such as SUPREM are capable of modeling the process in the bulk Si, the modeling of multilayer structures above the bulk substrate is still to be developed. This paper presents the first results showing this multilayer simulation capability. A typical NMOS structure involving multilayers is used as an example. Fig. 1 shows the cross section of a general NMOS including shallow $n^+$ junction as well as regions which use polycrystalline silicon as a gate and buried contact material. The two vertical sections and the lateral properties of poly interconnects represent new technology features which are being characterized and modeled under support of this contract.

The experimental efforts involving polycrystalline silicon diffusion sources initiated a test structure effort using phosphorus-doped poly layers. The objective of the experiments is to obtain diffusion related parameters for phosphorus both in the bulk and polycrystalline layer. Moreover, in a multilayer environment as typical of current MOSFET technologies with polysilicon gates and buried contacts, the interaction of oxidation, segregation and diffusion in all regions of the simulation space is a critical factor. The structure used to investigate the poly effects is shown in Figure 2 and is basically an outgrowth of similar structures used to characterize OED effects in the oxide-bulk system.

Simultaneous measurement of spreading resistance profiles in all regions provide a quantitative means to compare adjacent profiles. The nitride-masked region allows neutral ambient conditions and the thin buffer oxide regions makes it possible to investigate phosphorus penetration through gate masks. Preliminary results of junction depth data as a function of diffusion time are shown in Figure 3.

The results from the work on poly diffusion have shown that the point defects generated at the $Si-SiO_2$ interface during oxidation are partially transmitted to the substrate to enhance phosphorus diffusion into the bulk. The OED however, is less than that observed for only bulk OED. It is thought that part of the Si interstitially generated at the oxidizing interface recombine with the vacancies at grain boundary as they diffuse along the grain boundary. Such hypothesis is to be further investigated to establish a better model of the interaction between grain boundary and Si interstitials.

The work involving grain growth in polycrystalline Si is progressing to determine the grain growth mechanism at different thermal process conditions and doping conditions of poly. Extensive experiments using transmission electron microscope have been done to characterize the grain size and crystalline structure of poly. During thermal processing, the average grain size of poly layers increases proportional to the square root of time. The grain growth is thought to be a diffusion controlled mechanism [1], where the presence of impurities plays two roles: 1) the increase of vacancy concentration due to the shift of Fermi level and, 2) the change of grain boundary energy due to impurity segregation at grain boundaries. In general, As and P doping show a variable degree of

enhancement on the grain growth while B doping has little effect. The As doped poly, for example, shows an initial increase in the grain size with the increase of concentration beyond $1 \times 10^{19}$ atoms/cm$^3$. However enhanced grain growth reaches a maximum and decreases for higher concentrations. The initial increase in grain size is due to the increase in vacancy concentration at higher doping concentration levels. However, when the solid solubility is exceeded, the vacancy concentration does not increase further. Rather, the segregated impurities at grain boundary lower the grain boundary energy as well as the presence of clusters increases the resistance of boundary migration, thus contributes to the reduced growth rate. The activation energy of grain growth varies for different dopant concentrations. The apparent activation energy is the sum of those of various processes: vacancy formation, self-diffusion of Si, grain boundary segregation as well as the cluster formation. Depending on the relative importance of each process at a given process condition, the activation energy varies accordingly.

C. SUPREM Development

During the initial period of this contract the groundwork for implementing SUPREM III was initiated -- careful consideration was given to implementation of oxidation and epitaxial growth models. While it is desirable to have model upgrade capabilities with SUPREM II, certain constraints in Version II preclude model changes. Model coefficient array limitations as well as user interface considerations concerning inputting and modification of data -- oxidation data in particular -- require extensive changes to the existing program structure.

Two major activities concerning SUPREM III were initiated during this contract period. A working model for crystallization and conductivity modeling of polycrystalline layers was developed including results of Mandurah concerning carrier segregation. This model will form the basis for an implementation of multilayer structures in SUPREM. The second activity involved the initial efforts in implementing the SUPREM III data structures and model processing routines. This effort will continue through the remainder of this contract. An example of the model capabilities for multilayer polycrystalline structures is shown in Fig. 4. This figure shows the results of experiments involving interactions of grain growth on changes in sheet resistance for a range of experimental conditions. Fig. 4 shows both simulated and experimental results for phosphorus doped poly annealed at 950°C for three hours.

D. Interactions with Industrial Users of SUPREM

The interactions with industrial users of Stanford-developed process models and modeling programs have been substantial during this period. Two SUPREM-forums were held as well as the Annual Review. Each of these meetings is now briefly reviewed.

A total of 80 people attended the SUPREM Users Forum on February 11, 1980 and more than 52 companies were represented. Major highlights of the feedback and discussion involved:

1. Strong interest in all new oxidation and related diffusion models.
2. Interest in greater user freedom to adopt models and data to local needs.
3. A desire to form local user-groups and possibly generate round-robin test structures to benchmark results and coefficients.
4. Encouragement to enhance coupling of SUPREM and SEDAN and even include more capabilities in SUPREM for electrical calculations such as pinched resistance and threshold voltage.

A European SUPREM Users Forum was held on March 21, 1980 and R. W. Dutton attended as the Stanford representative. A detailed list of attendees and summary comments are attached as Appendix I. Several especially relevant comments concerning this program involve proposed user "fixes" for oxidation models. Subsequent visits to the Siemens and IFT Laboratories in Germany added new insight into alternative modeling approaches especially suited for high concentration diffusion and ion implanted profiles.

The annual review was held on July and as a result there were extensive interactions with industrial users of SUPREM. Appendix II shows the program as well as samples from user feedback indicate that the format and context of the meeting matches well with needs and expectations of our industrial counterpart. All current updates for SUPREM II version 0.5 have been completed and results were distributed at the meeting. The GEMINI (formerly TANDEM) program was completed and prepared for release. As indicated in the Appendix, the entire second day of the July meeting was devoted to review and discussion of all simulators (SUPREM, SEDAN and GEMINI).

E. Device Analysis Based on SUPREM Process Models

As indicated in the previous section, the device analysis capabilities developed under the previous contract DAAB07-77-C-2684 were completed and distributed during this period. Two aspects of this work are summarized below:

1) two dimensional MOS device analysis,

2) one-dimensional semiconductor device analysis (SEDAN)

An intensive effort was directed toward completion of device modeling activities. The analysis results using the Poisson solution program GEMINI

were benchmarked against the CADDET program and a novel equation set for computing currents was shown to be accurate to better than 40% over more than six decades of current [2]. Results using the boundary value method for numerical analysis have now shown explicitly the short channel transient charge effects of velocity saturation and substrate doping. Previous published predictions of speed limits apply only for slow transients and light substrate doping. The simulations have been confirmed experimentally for long channel test structures and using analytical model calculations [3].

The SEDAN program was released during this contract period. The program provides an effective coupling of 1-D process modeling into a counterpart device analysis capability. Applications for both MOS and bipolar devices have been considered by industrial users. At present the internal activities have shifted to 2D MOS analysis. Hence the active support and further development of SEDAN will depend on new contract support.

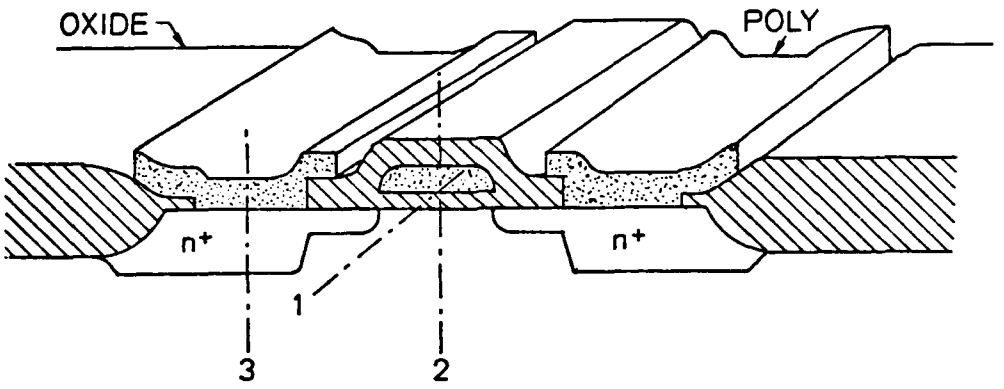


Fig. 1. The cross-sectional view of a typical NMOS structure showing three features of simulation examples.

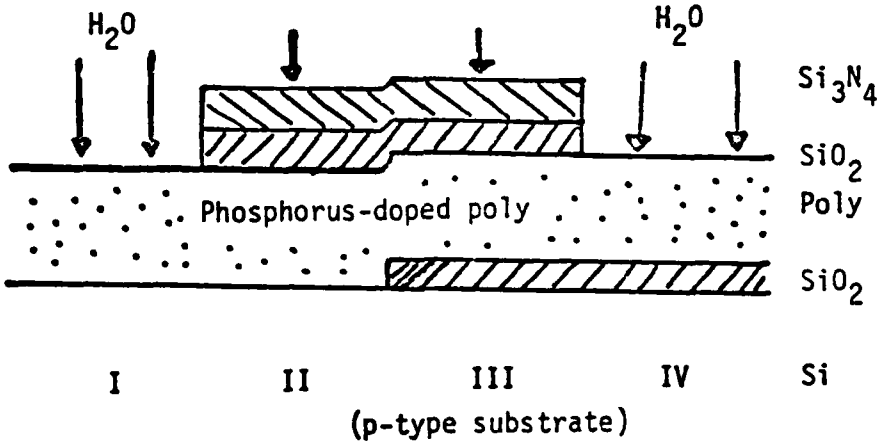


Fig. 2. Cross-section showing polycrystalline diffusion sources for phosphorus into bulk silicon. Regions I and II are directly contacted to the bulk and regions III and IV are over a thin oxide. In regions II and III the poly is covered with nitride to prevent oxidation.

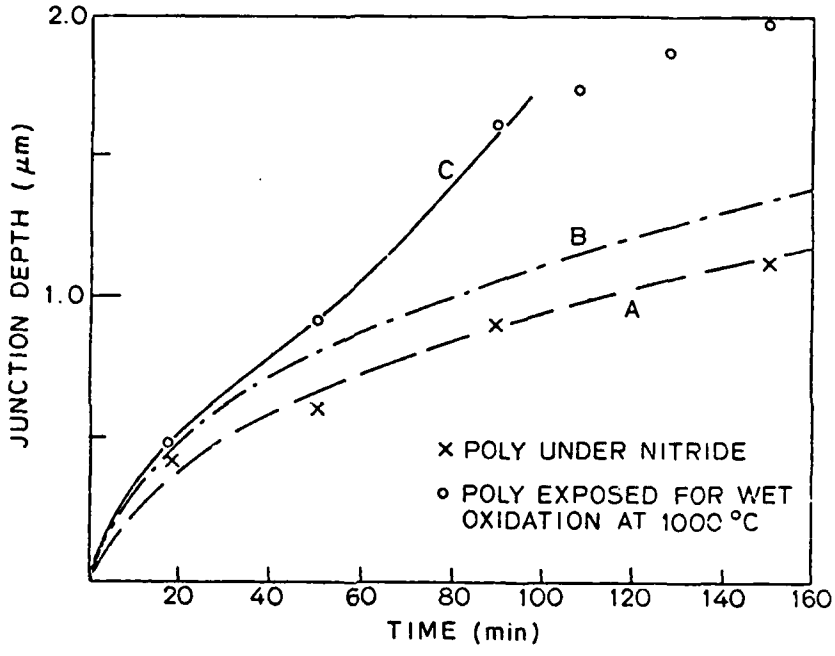


Fig. 3. The junction depth as a function of diffusion time of cross section 3 in Fig. 1. Experimental data are for both annealing and oxidation. Curve B is the simulated result without including the OED effect.

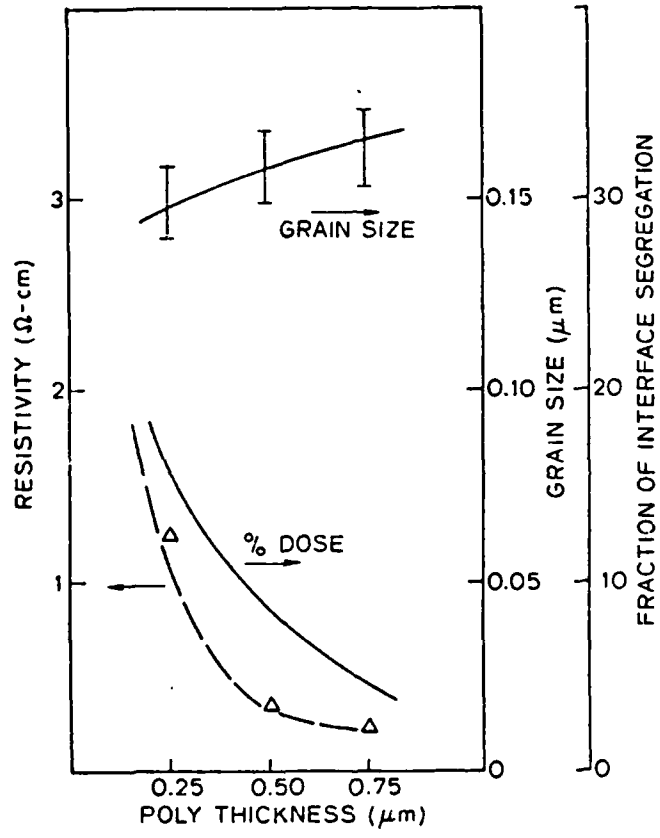


Fig. 4. The resistivity, grain size and fraction of interface segregation as functions of poly thickness.

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Appendix I

SUPREM

March 21, 1980

Forum held at Universite Catholique de Louvain

Appendix I

DATE: April 1, 1980

TO : DARPA/MATS Process Modeling Group

FROM : Bob Dutton

SUBJECT: SUPREM Forum at Universite Catholique de Louvain

Attached is a list of attendees for the SUPREM User Forum held at UCL on March 21, 1980. In the discussion of SUPREM results the following points of interest were raised:

- Enhanced oxidation for heavy doping should not increase infinitely with 1/T and a user's fix was proposed by Kuisl from AEG.

- Kuisl and others were very interested in thin oxides and have already implemented Blanc's model (APL, Sept. 1978) in SUPREM.

- In addition Kuisl proposed a further fix for HCl:

$$\alpha = \alpha_T \ (1 + \alpha_1[HCl])$$

$$\beta = \beta_T \ (1 + \beta_1[HCl])$$

where the $\alpha$ and $\beta$ coefficients are modified in Blanc's model.

- Interest in Phosphorus deposition and diffusion is reasonably high in Europe, obviously for the bipolar designers. The group from CNET (Lescronier) have some interesting data on cooperative P-B effects (see attached). Both SGS (Ferla) and Philips (Jansen) had comments on phosphorus parameters and modeling. STL (Scovell) presented data on phosphorus results as well.

- Cooperative As-B effects were discussed by IFT (Ryssel) and RTC (Brebisson). The IFT group has developed their own program ICECREM and the results will appear in the August 1980 VLSI issue. The necessary changes will be made in SUPREM to include the IFT approach. This was well received by participants since the overall capabilities of ICECREM are limited to implantation and diffusion.

- There was substantial interest in having better $\rho$ and $V_T$ capabilities directly in SUPREM. In addition it was suggested to allow more general LOAD capabilities so that measured profiles can be inputted for further simulation.

FACULTÉ DES SCIENCES APPLIQUÉES

LABORATOIRE DE MICROÉLECTRONIQUE

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UNIVERSITÉ CATHOLIQUE
DE LOUVAIN

*PROCESS MODELING WORKSHOP*

*UNIVERSITE CATHOLIQUE DE LOUVAIN - Laboratoire de Microélectronique -*

*Le 21 mars 1980*

## *LIST OF PARTICIPANTS*

- *Mr. de BREBISSON - R.T.C. - Caen (France)*
- *Mr. H. RYSSEL - I.F.T. - München (Deutschland)*
- *Mr. P. SCOVELL - S.T.L. - Harlow (Great Britain)*
- *Mr. R. W. DUTTON - Stanford University - Stanford (U.S.A.)*
- *Mr. M. KUISL - AEG Telefunken - Ulm (Deutschland)*
- *Mr. DAUBONNE - Motorola - Toulouse (France)*
- *Mr. BAYLAC - E.F.C.I.S. - Grenoble (France)*
- *Mr. MORIN - E.F.C.I.S. - Grenoble (France)*
- *Mr. MADAS - Siemens - München (Deutschland)*
- *Mr. GANSNER - Ecole Polytechnique Fédérale de Lausanne - Lausanne (Suisse)*
- *Mr. JANSEN - Philips - Eindhoven (Nederland)*
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- *Mr. VAN ISEGHEM - Bell Tel. Mfg - Antwerpen (Belgique)*
- *Mr. VANDORPE - Micado - Meylan (France)*
- *Mr. WEBB - Philips - Southampton (Great Britain)*
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- *Mr. FERLA - SGS-ATES - Milano (Italia)*
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- *Mr. DUTOIT - Centre Electronique Horloger - Neuchatel (Suisse)*
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- *Mr. OLIJSLAGERS - TH Eindhoven - Eindhoven (Nederland)*
- *Mr. MATTHEUS - Bell Tel. Mfg - Antwerpen (Belgique)*

./.

- Mr. SUCKOW - Valvo - Hamburg (Deutschland)
- Mr. KOERSELMAN - Philips - Nijmegen (Nederland)
- Mr. KRANZER - Siemens - München (Deutschland)
- Mr. BRAND - Philips -Nijmegen (Nederland)
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- Mr. DE LA SALLE - I.B.M. - Corbeil Essonne (France)
- Mr. SCHUTZ - Technical University of Vienna - Wien (Austria)
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- Mr. BROSSELAAR - E.S.I.E.E. - Paris (France)
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- Mr. DEMOULIN - U.C.L. - Louvain-la-Neuve (Belgique)
- Mr. JESPERS - U.C.L. - Louvain-la-Neuve (Belgique)
- Mr. VAN de WIELE - U.C.L. - Louvain-la-Neuve (Belgique)
- Mrs. TRULLEMANS - U.C.L. - Louvain-la-Neuve (Belgique)

Appendix II Stanford University Announces a Two-Day Program

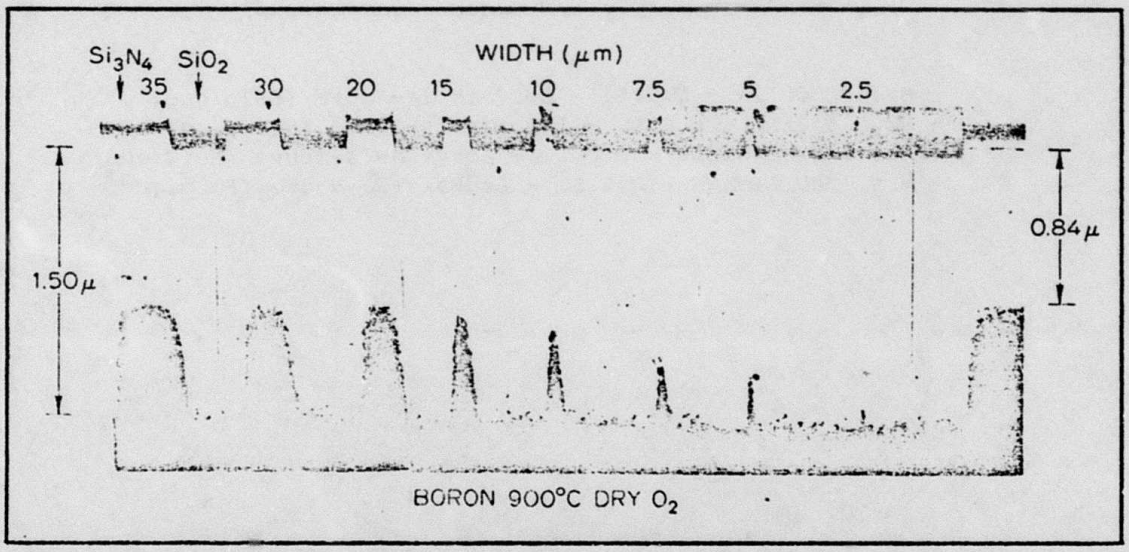
# Computer-Aided Design of IC Fabrication Processes

## Technology Modeling

Monday July 7, 1980

## Process and Device Simulation

Tuesday July 8, 1980




Stained junction profiles for a test structure used to characterize the two dimensional nature of oxidation enhanced diffusion of Boron in Silicon.

# Computer-Aided Design of IC Fabrication Processes

A two-day program: July 7-8, 1980 Stanford, California

The 1980's will be the era of production submicron silicon technologies. This will entail stringent process control requirements for oxides, impurity profiles and metallization. The purpose of this two-day meeting is to: 1) explore the fundamental processing steps involved in submicron technologies and 2) demonstrate how technology models can be used via computer simulation for device design and process control.

The meeting format will be a series of lectures as outlined in the program. Speakers will provide copies of foils. In addition, technical reports will be distributed which give an extended discussion of further background and details of the experiments, models and computer programs. The registration fee includes all course materials as well as lunches. The first day will involve primarily lectures and discussions of the materials aspects of technology modeling with substantial emphasis on specific experimental and model results. The second day will focus on more general aspects of simulation programs such as SUPREM and TANDEM. A "forum" atmosphere will be encouraged to obtain specific user feedback. A number of specific applications and results (case studies) will be presented.

Location: Terman Auditorium, Stanford University, Stanford, California.

Fee: The fee for each day is $125 (including lecture notes and luncheon) or $200 for attending both days. Enrollment is limited, and advance enrollment is required.

## Instructional Staff

NELSON N. CHAN, Member Technical Staff, Intel, Santa Clara, California

BRUCE E. DEAL, Manager, Fairchild R&D, Palo Alto, California

ROBERT W. DUTTON, Associate Professor, Stanford University

JAMES F. GIBBONS, Professor, Stanford University

JAMES A. GREENFIELD, Research Affiliate, Stanford University

CHARLES P. HO, Research Associate, Stanford University

CHARLES ROBERT HELMS, Adjunct Professor, Stanford University

THEODORE I. KAMINS, Member Technical Staff, Integrated Circuits Laboratory, Hewlett-Packard, Palo Alto, California

A. MIN-RON LIN, Research Affiliate, Stanford University

JAMES D. PLUMMER, Associate Professor, Stanford University

KRISHNA SARASWAT, Senior Research Associate, Stanford University

WILLIAM TILLER, Professor, Stanford University

## Technology Modeling

Monday July 7, 1980

| | | |
|---|---|---|
| 8:30 a.m. | Introduction | Dutton |
| 8:45 | Gate and Isolation Oxidation | |
| | Thin Oxides | Plummer |
| | High Pressure Oxidation | Deal |
| | Interaction of Oxidation with Other Processes | Tiller |
| 10:00 | Break | |
| 10:20 | Interconnection Technologies | |
| | Polycrystalline Silicon | Kamins |
| | Silicides | Saraswat |
| 11:30 | Lunch | |
| 1:00 p.m. | Impurity Profiles and Dopant Redistribution | |
| | Ion Implantation | Gibbons |
| | Diffusion | Lin |
| | Behavior of Impurities at Interfaces | Helms |
| 2:20 | Break | |
| 2:45 | Contact Technologies | |
| | Buried Contacts | Dutton |
| | Temperature Tolerant Metallurgy for Transient Process Characterization | Ho |
| 3:30 | Audience Discussion on Future Directions of Process Modeling | |

## Process and Device Simulation

Tuesday July 8, 1980

| | | |
|---|---|---|
| 8:30 a.m. | Introduction to Simulation | Dutton |
| 9:00 | Updates for SUPREM (version II.05) | Dutton |
| 10:00 | Break | |
| 10:20 | Discussion of Process Simulation Including User-Presented Problems† | |
| 11:30 | Lunch | |
| 12:30 p.m. | Program Demonstrations and Lab Tour | |
| 1:15 | One-Dimensional SEmiconductor Device ANalysis (SEDAN) and Applications | Chan |
| 2:00 | Break | |
| 2:20 | Two-Dimensional ANalysis for DEvice Modeling (TANDEM) and Applications | Greenfield |
| 3:00 | Discussion of Device Simulation Including User Experience and Needs | |
| 3:45 | Lab Session Based on User-Provided Examples | |

† Typical presentations include a few foils and five minutes of discussion.

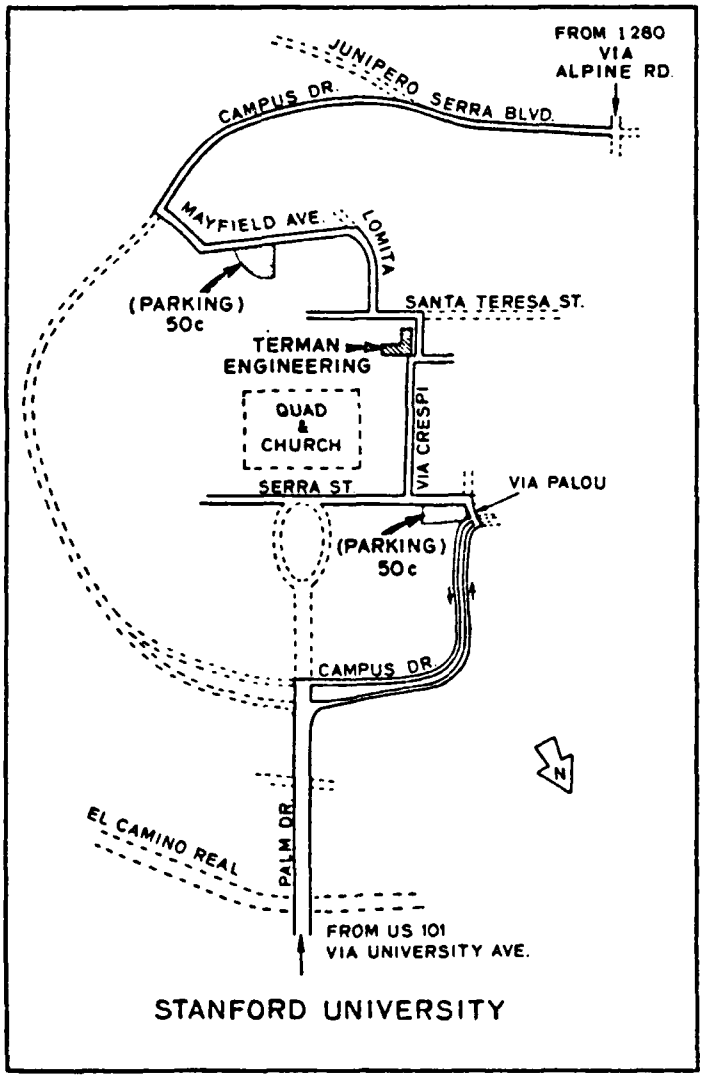
## General Information

**How to enroll:** Enrollment is limited and advance enrollment is required. Enrollment may be made by individuals or companies. Upon request, a place in the program will be reserved for individuals who require time to obtain authorisation.

**To enroll:** Please complete and return the form provided.

**Refunds:** If you enroll and then cannot attend, a refund, less $10 service charge, will be granted if requested in writing prior to the date of the program.

**For further information:** Write or call Stanford University Integrated Circuits Laboratory, c/o Robert Dutton, AEL Bldg, Stanford, California 94305; telephone (415) 497-1349.




(Enrollment is limited. Advance enrollment is required)

If enrolling more than one person, please enclose a separate sheet to give name, affiliation, address, and telephone number for others.

**Please mail to:** Stanford University Integrated Circuits Laboratory, c/o Robert Dutton, AEL Bldg., Stanford, California 94305.

I enclose a check in the amount of $_____ to cover _____ enrollment(s) in (check one):

| [ ]Technology Modeling | [ ]Process and Device Simulation | [ ]Both |
|---|---|---|
| July 7, 1980 | July 8, 1980 | |
| ($125) | ($125) | ($200) |

Name _____
last first middle

Employed by _____

Company address _____

_____
city state zip

Daytime telephone and extension _____

Make check payable to STANFORD UNIVERSITY.

Stanford University

Integrated Circuits Laboratory

Stanford, California 94305

# Computer-Aided Design of IC Fabrication Processes

A two-day program: July 7-8, 1980 Stanford, California